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FINAL REPORT

A STUDY OF LINEAR APPROXIMATION TECHNIQUES FOR SAR AZIMUTH PROCESSING

BY

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This work was performed for the Jet Propulsion
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RCA | Government Systems Division
Missile and Surface Radar
Moorestown, New Jersey 08057

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ABSTRACT

A study has been conducted of the application of the step transform subarray processing technique to synthetic aperture radar (SAR). The subarray technique permits the application of efficient digital transform computational techniques such as the fast Fourier transform (FFT) to be applied while offering an effective tool for range migration compensation. Range migration compensation is applied at the subarray level and with the subarray size based on worst case range migration conditions, a minimum control system is achieved.

A baseline processor was designed for a four-look SAR system covering approximately a 4096 by 4096 SAR sample field every 2.5 seconds. Implementation of the baseline system was projected using advanced low power technologies including 64K RAMs and CMOS/SOS arithmetic elements. A 20 km swath (one fifth of 100 km total) is implemented with approximately 1000 circuits having a power dissipation of from 70 to 195 watts.

The baseline batch step transform processor is compared to a continuous strip processor, and variations of the baseline are developed for a wide range of SAR parameters.

NEW TECHNOLOGY

No new technology developments were identified during the course of the study.

TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
1.0	INTRODUCTION	1
2.0	TECHNICAL DISCUSSION	2
2.1	SAR PROCESSOR SPECIFICATIONS	2
2.2	STEP TRANSFORM SUBARRAY PROCESSING ALGORITHM	6
2.2.1	Background	6
2.2.2	Step Transform Algorithm For Linear FM Pulse Compression	6
2.2.3	Step Transform Algorithm Applied To Synthetic Aperture Radar	11
2.2.4	Mathematical Analysis of Step Transform SAR Processor	13
2.2.5	Summary of Step Transform Processing Factors	23
2.3	BASELINE PROCESSOR DESIGN STUDY RESULTS	26
2.3.1	Baseline SAR System Design	26
2.3.1.1	System Parameter Definition	26
2.3.1.2	Performance Level of Baseline System	33
2.3.2	Implementation of Baseline System	39
2.3.2.1	Baseline SAR Processor Design	39
2.3.2.2	Semiconductor and Memory Technology	42
2.3.2.3	Memory Implementation	44
2.3.2.4	Pipeline FFT's	46
2.3.2.5	Hardware Summary	53
2.4	ALTERNATIVE PROCESSOR STUDY RESULTS	55
2.4.1	Variations of SAR Radar Parameters on Subarray Processing	55
2.4.2	Variations in Implementation of Step Transform Processing	58
2.4.2.1	General Programmability of Step Transform Processor	58
2.4.2.2	Multi-Look Batch Versus Continuous Strip Processing	61
3.0	STUDY RESULTS, CONCLUSIONS AND RECOMMENDATIONS	69
	LIST OF REFERENCES	71

LIST OF ILLUSTRATIONS

<u>FIGURE</u>	<u>TITLE</u>	<u>PAGE</u>
1	Step Transform Linear FM Matched Filter	7
2	Correlation of Linear FM Signal and Reference	8
3	Correlation of Linear FM Signal with Multiple References To Minimize Energy Loss	9
4	Reduction of Redundant Correlations	10
5	Repeated Spectrum Analysis of Short Time Apertures	10
6	Subarray Synthetic Aperture Processing	11
7	Platform Motion Compensation	13
8	Array Processing with Continuous Reference	15
9	Representation of Continuous Reference Output	15
10	Subarray Processing Parameters	16
11	Effect of Overlap on Aliasing in Second FFT Response	19
12	Two Dimensional Frequency Plane	21
13	Region of Interest for Output Points	21
14	Practical Implementation of Step Transform Matched Filter	24
15	Practical Implementation of Step Transform Matched Filter (Continued)	24
16	Baseline SAR System Parameters	27
17	Resolution Element Motion Relative to Fixed Antenna	28
18	Rotational Range Walk Between Subarrays	31
19	Multilook Registration	32
20	Uncompensated Range Walk Effects	34
21	Integrated Range Cell for Baseline System (Compared to Ideal Gaussian)	37
22	Integrated Range Cell for Max. $R_D=0.5$, Max. $R_r=0.5$ (Compared to Ideal Gaussian)	38
23	Block Diagram of Azimuth Processing Functions	40

LIST OF ILLUSTRATIONS (CONTINUED)

<u>FIGURE</u>	<u>TITLE</u>	<u>PAGE</u>
24	Implementation of Step Transform Subarray SAR Processor 20 km Swath	41
25	Power Delay Product Comparisons	43
26	Memory Chip Capacity Trends	44
27	Corner Turning Memory	45
28	Single Memory Corner Turning	45
29	Subarray Formation	47
30	6 Stage Pipeline FFT Functions	51
31	Floating Point Radix-2 FFT Stage	52
32	Block Diagram of Azimuth Processing Functions with 2 Pre-Filters	57
33	Programmability of Baseline Processor Design	59
34	Multi-Look Spectrum Coverage	63
35	Continuous Strip Multi-Look Processor	64
36	Diagonalization of Corner Turning Memory for Continuous Strip Map Processor	66
37	Continuous Strip Memory Read-Out Sequence	67

LIST OF TABLES

<u>TABLE</u>	<u>TITLE</u>	<u>PAGE</u>
1	SAR System Parameters	3
2	Processor Requirements for Various Missions	4
3	SAR Processor Performance Requirements	5
4	Preferred Ranges of Design Parameters	5
5	Sample Unweighted Response Case, No. 1 and 2	22
6	Baseline SAR Processing Parameters	29
7	Memory Requirements (20 km Swath)	48
8	Transform Alternatives	49
9	FFT Options	50
10	Radix-2 FFT Stage Circuit Counts, Excluding Control	53
11	Baseline On-Board Hardware Summary - 20 km Swath	54
12	Subarray Constraints for Various Mission Requirements	56

1.0 INTRODUCTION

The formation of mapping images with a satellite borne synthetic aperture radar (SAR) presents challenging signal processing problems. Current processors are located on the ground and process the raw, unprocessed data transmitted from the spacecraft (S/C) in non-real time. That is, images can be formed from only a small portion of the total radar returns. A need, therefore, exists for a SAR signal processor which can operate on the radar data in "real" time and thus provide imagery from the total swath scanned by the radar. In addition, the wide bandwidth, unprocessed signal places great demands on the communication link. Typical SAR processors use multiple looks at an image field to reduce speckle effects and thus improve image quality. This multiple look processing reduces the required bandwidth of the processed SAR data by a factor equal to the number of looks integrated. If the multiple-look processing could be done on board the S/C, a similar reduction would be realized in the communication link requirements.

This report summarizes the results of a broad feasibility study of the application of step transform subarray techniques to azimuth processing of SAR data acquired by earth satellites. The study has comprised two major parts, 1) the conceptual design of a processor meeting the requirements of baseline SAR system parameters; and 2) the adaptations of the baseline design required by variations in radar parameters. The baseline system parameters and variations were provided by JPL.

The material presented follows the sequence: general requirements (2.1), general analysis of step transform algorithm for SAR applications (2.2), development of baseline SAR processing parameters and implementation (2.3), and the effect of variations in SAR parameters (2.4). Conclusions and recommendations for future SAR processor development have been provided.

2.0 TECHNICAL DISCUSSION

2.1 SAR PROCESSOR SPECIFICATIONS

The baseline SAR processor has been designed to meet the functional requirements associated with the SAR system characterized by the parameters listed in Table 1. An objective of the baseline design is to achieve an architecture which enables a variety of SAR system requirements to be met by the same basic functional elements which would be individually programmed for each case. The types of radar parameter variations which have been considered are given in Tables 2 and 4.

Required performance levels for the processor are given in Table 3.

The baseline processor design has been configured with the ultimate goal of on-board processing. Thus the implementation has emphasized low power, weight, and size as required. No parts have been employed in the baseline design which can be ruled out for an earth satellite environment.

Specific interface definitions include the following:

- Input SAR Data:
 - Range Compressed
 - Digital, Sampled Data
 - Quantization, 6 Bits I and 6 Bits Q
- Output SAR Image Data:
 - Magnitude Squared
 - Quantization Level, 8 Bits
- Input Control Parameters:
 - PRF
 - S/C 3-Space Coordinates
 - Antenna Look Angle
 - Doppler Center Frequency
 - Chirp Rate
 - (Nominal values can be inferred from Table 1)

TABLE 1. SAR SYSTEM PARAMETERS

<u>PARAMETER</u>	<u>NOMINAL VALUE</u>
S/C Altitude	800 km
S/C Speed	7.5 km/sec
S/C Orbit Semimajor Axis	7168.3 km
Orbit Eccentricity	0.001
Argument of Perigee	90°
Orbit Inclination	108°
Earth Equator Radius	6378.4 km
Earth Polar Radius	6356.9 km
Dynamic Range, Point Target	50 dB
Dynamic Range, Distributed Target	20 dB
Roll	$\pm 0.5^\circ$
Antenna Pitch	$\pm 0.5^\circ$
Yaw	$\pm 0.5^\circ$
Look Angle	20°
Transmitter Frequency	L-Band (1275 MHz)
PRF	1645 Hz
Swath Width	100 km
Antenna Width	2.16 m
Antenna Length	10.5 m
Range Pulsewidth	33.8 Microseconds
Range Bandwidth	19 MHz
Total Integration Time	2.5 Sec

TABLE 2. PROCESSOR REQUIREMENTS FOR VARIOUS MISSIONS

<u>RESOLUTION</u>	<u>SWATH WIDTH</u>	<u>AZIMUTH LOOKS</u>	<u>RANGE LOOKS</u>	<u>TRANSMITTER FREQ. BANDS</u>	<u>INCIDENCE ANGLE</u>	<u>SIDELOOKING ANGLE</u>
10 m	10 km	1	1	L,C	25°	90°
50 m	100 km	8	1	L	65°	90°
50 m	50 km	8	2	L	25°	45°
50 m	50 km	8	2	L	25°	90°
75 m	185 km	4	1	C	25°	90°
200 m*	100 km	32	1	L	49°	90°

* S/C Altitude - 375 km

NOTE: L-Band is 1275 MHz

C-Band is 5280 MHz

TABLE 3. SAR PROCESSOR PERFORMANCE REQUIREMENTS

Resolution (3 dB) (Both Range and Azimuth)	≤ 25 meter
Number of Looks in Range	1
Number of Looks in Azimuth	4
Signal to Noise Ratio Within 3 dB Mainlobe	12 dB

TABLE 4. PREFERRED RANGES OF DESIGN PARAMETERS

<u>PARAMETER</u>	<u>INTERVAL OF INTEREST</u>
Resolution, Range and Azimuth	10 m to 200 m
Swath Width	10 km to 400 km
Number of Range Looks	1 to 4
Number of Azimuth Looks	1 to 64
Transmitter Frequency Bands	L, S, C, X, K, V
Dynamic Range of Target Response	25 dB to 100 dB
Incidence Angle	15° to 65°
Sidelook Angle	45° to 135°
S/C Altitude	275 km to 1200 km

2.2 STEP TRANSFORM SUBARRAY PROCESSING ALGORITHM

2.2.1 Background

A key technical problem in processing of SAR data for imagery is range migration during the radar imaging time. Range migration will occur both within and between separate "looks" at an image field. Correction for range migration effects can be accomplished to a very high degree of precision by treating each received radar sample effectively independently in the synthesis of the desired image. However, this approach also requires a maximum number of implementation functions and a large control signal field. A signal processor under development at JPL^(1,2) provides an efficient approach to implementing a totally programmable SAR image processor. It provides a highly modular implementation and minimizes the range migration control field by matching it to the actual migration. By employing very large scale integrated (VLSI) circuit techniques (one circuit per beam) the disadvantage of the need for N^2 operations to form an N element image line is alleviated. The system being developed uses CCD technology in the implementation of the VLSI circuit.

Another approach to range migration compensation is to break the synthetic array samples into segments, or subarrays, which are matched to the range migration. This approach has been called the step transform by RCA and was originally applied to linear FM radar waveform processing as a means of minimizing the size of a programmable digital matched filter.

A description of the step transform algorithm as applied to linear FM pulse compression and SAR is given in the following paragraphs.

2.2.2 Step Transform Algorithm For Linear FM Pulse Compression

The step transform algorithm provides an efficient method to perform pulse

compression of linear FM type waveforms. This algorithm can reduce the hardware requirements by up to 50% of conventional FFT approaches.

A block diagram of the linear FM step transform matched filter is shown in Figure 1. A short duration reference is mixed with the incoming signal and the output is fed to a Fast Fourier Transform (FFT) processor the time aperture of which is equal to the duration of the reference waveform but is less than the total waveform length. The output of the FFT is stored in a memory adequate in size to hold the full waveform. The samples are reordered and then passed to a second short aperture FFT the output of which represents the pulse compression of a linear FM signal. High speed FFT processing can be obtained using pipeline processing techniques and high-speed digital logic to provide a continuous pulse compressed output.

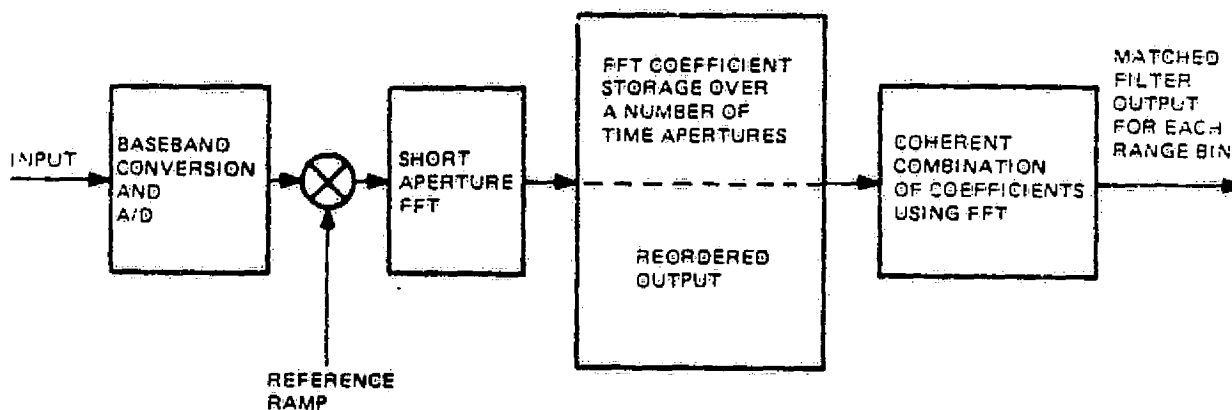


FIGURE 1. STEP TRANSFORM LINEAR FM MATCHED FILTER

The concept of the step transform can be understood by first referring to Figure 2.

This figure shows a time-frequency plot of a linear FM signal received at an arbitrary time, Δ , relative to a fixed reference linear FM. Mixing these two waveforms results in a CW signal the frequency of which is proportional to Δ and which exists over the period of time that the signals overlap. As Δ increases, the amount of overlap decreases, resulting in an output energy loss, a decrease in resolution, and an increase in collapsing loss.

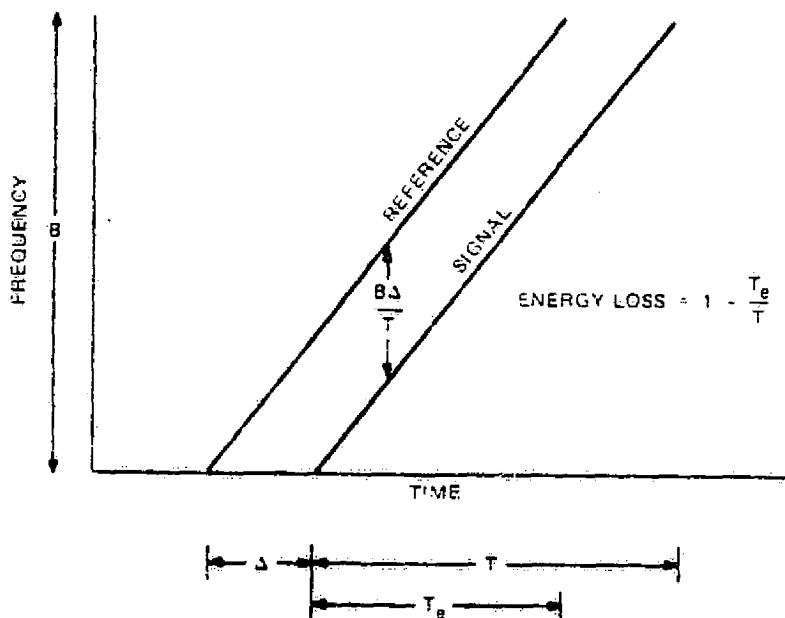


FIGURE 2. CORRELATION OF LINEAR FM SIGNAL AND REFERENCE

These losses can be reduced by using additional reference signals which are spaced closely together, as in Figure 3. Each reference covers only a small

region of incremental range delay and is mixed with the signal to produce output frequencies proportional to the time displacement of the references and the signal. During any increment of time that two references overlap the outputs of the mixers are identical with the exception that they are displaced in frequency.

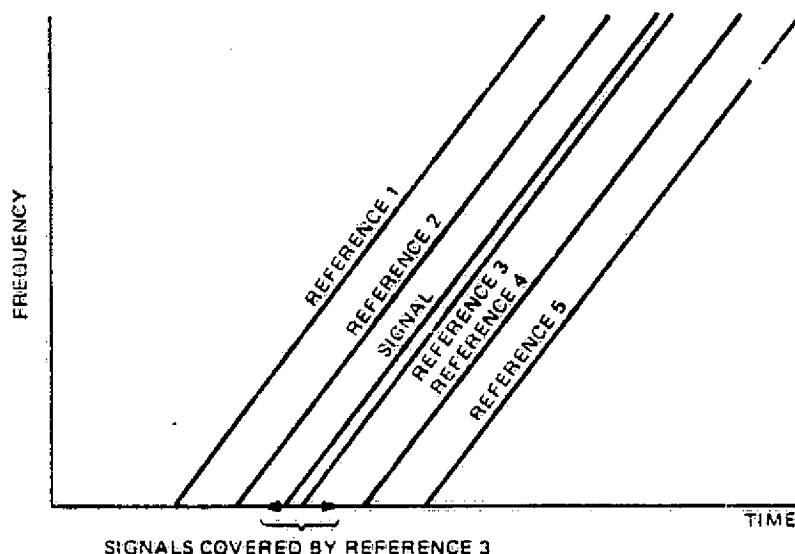


FIGURE 3. CORRELATION OF LINEAR FM SIGNAL WITH MULTIPLE REFERENCES TO MINIMIZE ENERGY LOSS

The multiple references can be replaced by a single sawtooth reference (shown in Figure 4) with no loss in information. When the sawtooth frequency reference is mixed with the linear FM signal, a step frequency function results (Figure 5). A short aperture FFT is used to measure the frequency of each step. This spectrum analysis starts at the beginning of the short reference ramp and stops at its

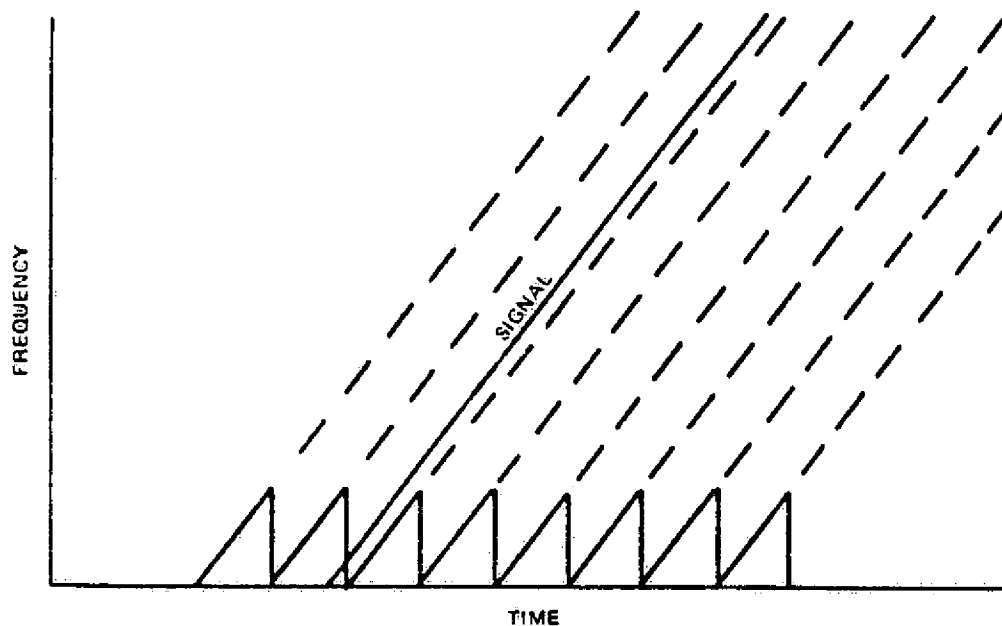


FIGURE 4. REDUCTION OF REDUNDANT CORRELATIONS

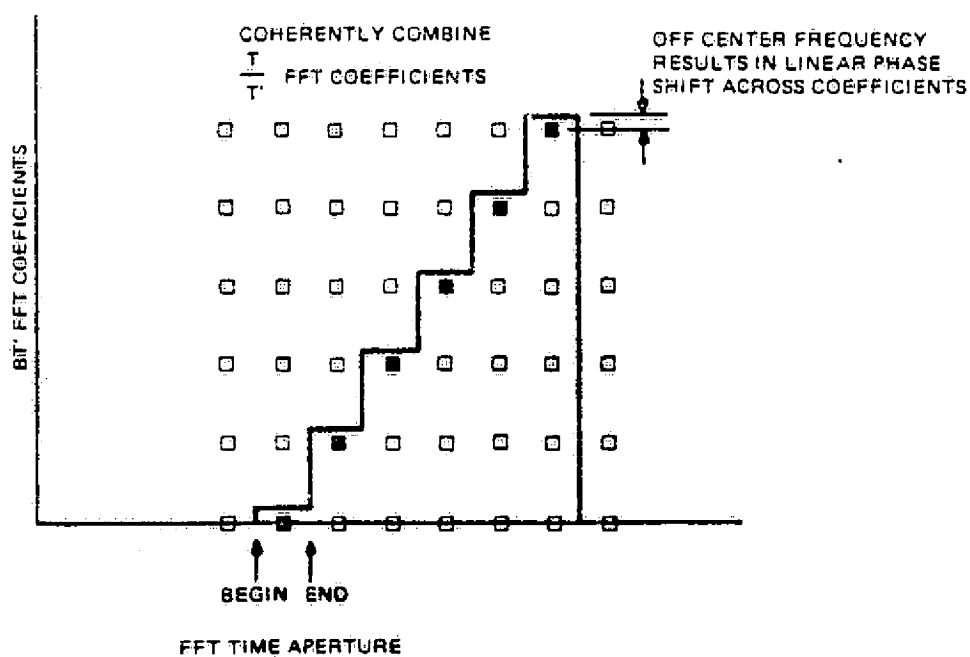


FIGURE 5. REPEATED SPECTRUM ANALYSIS OF SHORT TIME APERTURES

end. The resolution of the spectrum analyzer corresponds to the reciprocal of the time duration of the short ramp. The corresponding resolution is less than that of one range bin for a mixed linear FM signal. However, full resolution can be achieved by coherently combining successive spectrum analysis outputs over the waveform duration.

2.2.3 Step Transform Algorithm Applied To Synthetic Aperture Radar

In performing the azimuth processing for a focused synthetic aperture system, the range (or phase) pattern of pulse returns are matched to that which an azimuth element would follow due to the motion of the radar vehicle. The more pulses which are combined or the larger the length of the synthetic array, the higher the azimuth resolution.

The step transform process can be considered as a subarray approach to SAR processors, as shown in Figure 6. Each wide beam subarray can be focused toward the same azimuth element; the subarrays then can be combined to obtain the high angular resolution corresponding to that of the full aperture. In performing this operation, it is also necessary to overlap subarrays to avoid the grating lobes that would result if the subarrays were end to end.

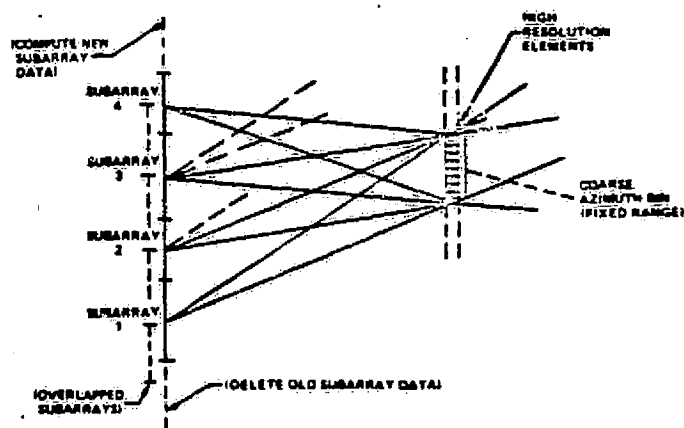


FIGURE 6. SUBARRAY SYNTHETIC APERTURE PROCESSING

As the full aperture is moved in space, each subarray changes its relative position in the aperture and a different beam position is required for combining with the other subarrays.

Since all subarray beam positions are used as it moves through the aperture, these beam positions can be computed as soon as the subarray data have been accumulated.

Figure 6 shows how the subarray beam positions are selected to cover a common azimuth coarse resolution element. Beam positions from subarrays 1, 2, 3, and 4 are shown overlapping at the same coarse azimuth bin. Each subarray requires a different beam position. If the new data are being obtained by subarray #3, its bottom beam position would be used while the other beam positions for subarray #3 are stored until needed. After a beam position has been used for each subarray, that beam position is not used again; therefore, it is not necessary to continue to store that data.

Figure 6 also shows the combining of the four subarrays to resolve the coarse resolution element to a number of high resolution elements. The above process then can be repeated, shifting the subarrays, to obtain the next set of contiguous high resolution elements.

Platform motion and range migration can be compensated for using the subarray approach by incorporating a range correction when combining the subarray outputs. This procedure is shown in Figure 7. As new subarrays are added and each subarray moves along the full aperture distance, the correction factor for the subarray is modified to match the actual flight geometry.

A synthetic aperture processing procedure using subarrays can be summarized as follows:

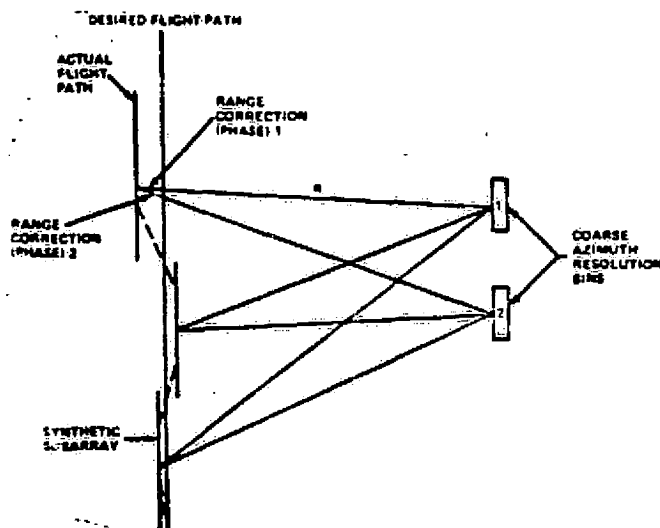


FIGURE 7. PLATFORM MOTION COMPENSATION

1. Focus data over short subarray time.
2. Store subarray data over large array length.
3. Combine subarray outputs to form large array.
4. Compute new subarray data entering large aperture.
5. Drop old subarray data leaving large aperture.

The implementation of the process is identical in principle to the range pulse compression except that pulse-to-pulse samples of the same range bin are applied for the azimuth processing.

2.2.4 Mathematical Analysis of Step Transform SAR Processor

A revised analysis of the step transform process has been conducted for this study. A previous analysis⁽³⁾ was modeled after the linear FM pulse compression case and did not provide a closed form expression for the output function.

Input Signal

The input to the coherent SAR processor from a point target consists of samples of a linear FM signal of the form $Ae^{ja'(t+t_0)^2}$. The purpose of processing is to measure the amplitude A and the offset t_0 .

Let $1/T$ be the prf. Then the samples are:

$$Ae^{ja(n+n_0)^2}, n = 0, 1, \dots, N-1 \quad (1)$$

where $a = a'T^2$, $n_0 = t_0/T$, and N is the number of samples in the array.

For the purposes of the SAR analysis, it is assumed that range migration compensation has been inserted. The means of handling range migration are included in Section 2.3.1.

Processing By FFT

Using a straight-forward FFT approach, the input sequence is first mixed with a reference $\{e^{-jan^2}\}_{n=0}^{N-1}$:

$$Ae^{ja(n+n_0)^2} e^{-jan^2} = Ae^{jan_0^2} e^{j2an_0n} \quad (2)$$

The signals are shown in Figure 8. In (2), the first factor $e^{jan_0^2}$ does not depend on n and has constant magnitude. Let $\{X_k\}_{k=0}^{N-1}$ be the DFT of the signal $\{e^{j2an_0n}\}_{n=0}^{N-1}$. The amplitude of $\{X_k\}$ follows the envelope $|\text{Sin } an_0N / \text{Sin } (an_0 - \pi k/N)|$, and has a peak around $k=k^*$ where $k^* = \frac{an_0N}{\pi}$. Specifically,

$$k^* - \frac{1}{2} < \frac{an_0N}{\pi} \leq k^* + \frac{1}{2} \quad (3)$$

It can be seen from (3) that n_0 is measured within an accuracy of $\pm \frac{\pi}{2aN}$ (see Figure 9).

Processing By Using Subarrays (Step Transform)

For subarray processing, the signal of (1) is first mixed with M references, each of duration K and separated by L , as illustrated in Figure 10. The m^{th} reference ($0 \leq m < M$) is therefore $\{e^{-ja(n-mL)^2}\}$, $mL \leq n < mL + K - 1$. The

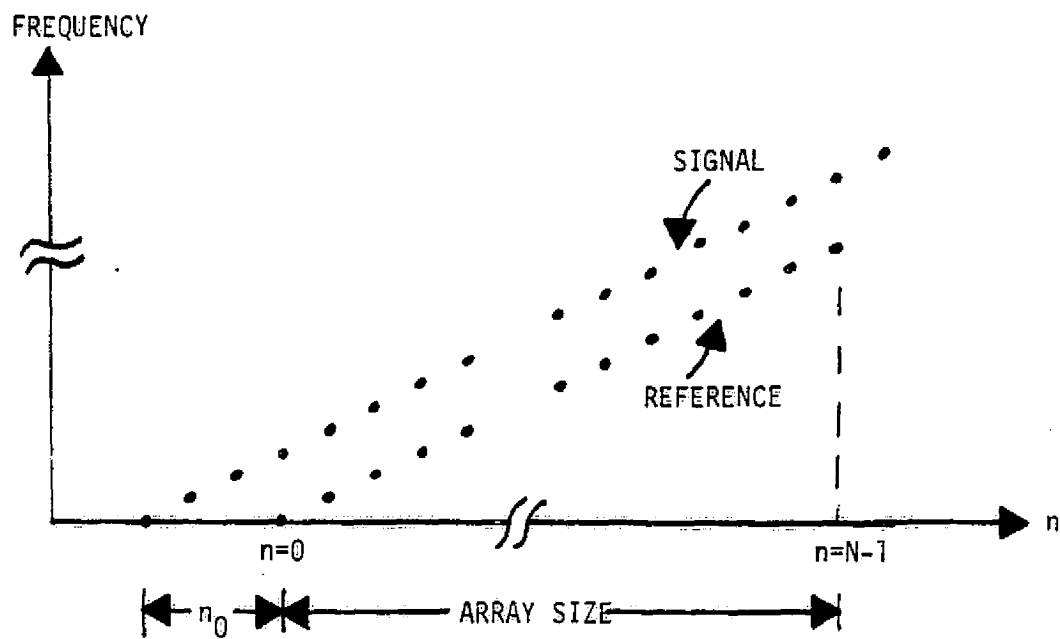


FIGURE 8. ARRAY PROCESSING WITH CONTINUOUS REFERENCE

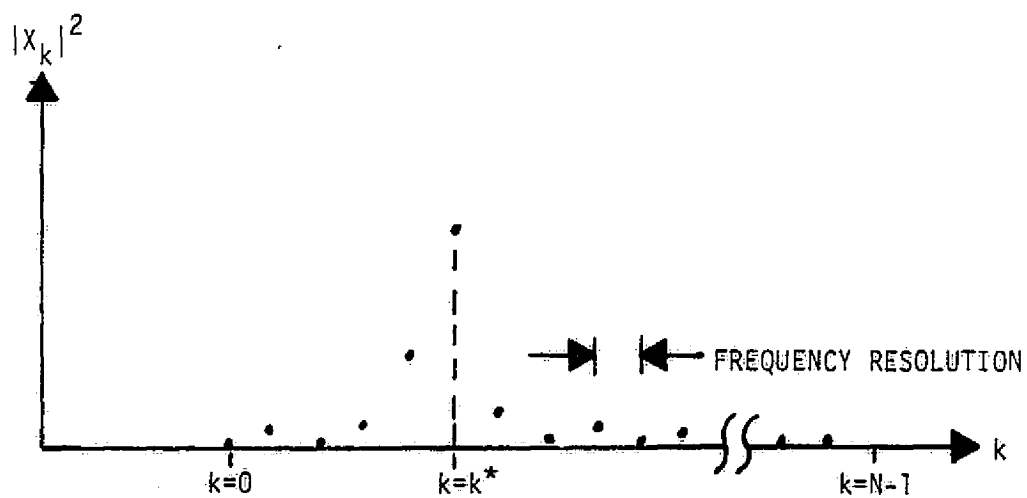


FIGURE 9. REPRESENTATION OF CONTINUOUS REFERENCE OUTPUT

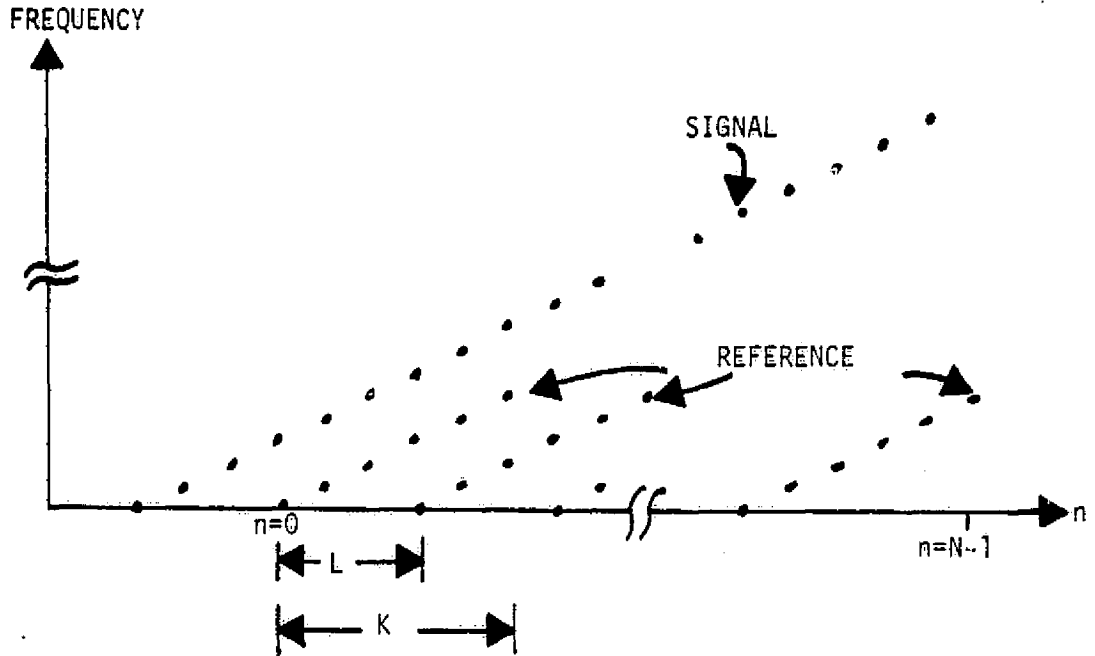


FIGURE 10. SUBARRAY PROCESSING PARAMETERS

result of this mixing is:

$$Ae^{j2\pi n' n_0} e^{j2\pi n' mL} e^{j\pi m^2 L^2} e^{j\pi n_0^2} e^{j2\pi n_0 Lm} \quad (4)$$

where $n' = n - mL$, $0 \leq n' \leq K - 1$. The factor $e^{j\pi m^2 L^2}$ is a known quantity and can be corrected for each of the m subarrays. The factor $e^{j\pi n_0^2}$ is constant for all m and n' with magnitude 1. The factor $e^{j2\pi n' mL}$ can be taken care of by mixing or a shift at the output of the first FFT. The important factors are the first, $e^{j2\pi n' n_0}$, and the last, $e^{j2\pi n_0 Lm}$.

Two FFT's are taken, the first is a K point FFT with n' as variable and m fixed, the second is an M point FFT with m as variable, but after a phase factor has been introduced.

Consider the K point signal $\{Ae^{j2\pi n_0 n'} e^{j2\pi n_0 Lm}\}_{n'=0}^{K-1}$. Its DFT is $\{A Y_k e^{j2\pi n_0 Lm}\}_{k=0}^{K-1}$, where $\{Y_k\}_{k=0}^{K-1}$ is the K -point DFT of $\{e^{j2\pi n_0 n'}\}$. Then $|Y_k| = |\sin(\pi n_0 K) / \sin(\pi n_0 (K-k))|$. The set $\{Y_k\}$ peaks around $k=k^*$ where

$k^* \approx \frac{an_0 K}{\pi}$. Or more precisely:

$$\frac{an_0 K}{\pi} = k^* + \zeta, \quad |\zeta| < \frac{1}{2} \quad (5)$$

From (5), it is seen that n_0 can be measured within an accuracy of $\frac{\pi}{aK}$, which, as expected, is considerably coarser than the accuracy of $\frac{\pi}{aN}$ in an N point FFT.

Suppose we now take an M point DFT of $\{AY_k e^{j2an_0 Lm}\}_{m=0}^{M-1}$ for each k . The factor which responds to this DFT is $e^{j2an_0 Lm}$. Let this DFT be $\{U_p\}_{p=0}^{M-1}$. Then $\{U_p\}$ peaks at $p = p^* \approx \frac{aLn_0 M}{\pi}$ and the accuracy with which n_0 can be measured is π/aLM , which is $\pi/a(N-K+L)$ and is very close to π/aN .

The results of the two stage FFT is a two dimensional array $\{AY_k U_p\}$, $0 \leq k \leq K-1$, $0 \leq p \leq M-1$. The value of $AY_k U_p$ corresponds to the frequency $\frac{2\pi}{K} k + \frac{2\pi}{LM} p$. The main peak is at $k = k^*$ and $p = p^*$, i.e., at frequency $\frac{2\pi}{K} k^* + \frac{2\pi}{LM} p^*$. However, the terms $AY_{k^*+1} U_{p^*}$ give rise to undesirable far grating lobes.

To suppress these grating lobes, we examine again the two dimensional array $\{AY_k e^{j2an_0 Lm}\}$, $0 \leq k \leq K-1$, $0 \leq m \leq M-1$. For each k , if it is indeed the k^* given by (5), then $n_0 \approx \pi k/aK$, and $2an_0 Lm \approx 2\pi Lkm/K$. So we take the M -point FFT of:

$$\{AY_k e^{j2an_0 Lm} e^{-j2\pi Lkm/K}\}_{m=0}^{M-1} = \{AY_k e^{j2aLm(n_0 - \pi k/aK)}\}_{m=0}^{M-1} \quad (6)$$

Let the DFT be $\{AY_k V_{p,k}\}_{p=0}^{M-1}$, where $\{V_{p,k}\}$ is the DFT of $\{e^{j2aLm(n_0 - \pi k/aK)}\}_{m=0}^{M-1}$.

Suppose $k=k^*$ which is given by (5). It is easy to show that:

$$|V_{p,k^*}| = \left| \frac{\sin(\pi \zeta LM/K)}{\sin[\pi(L\zeta/K - p/M)]} \right| \quad (7)$$

The set $\{V_{p,k^*}\}_{p=0}^{M-1}$ has a peak at $p=p^*$ where,

$$\frac{Lz}{K} = \frac{p^* + n}{M}, \quad |n| < \frac{1}{2} \quad (8)$$

Thus,

$$|V_{p^*, k^*}| = \left| \frac{\sin \left[\frac{(p^* + n)\pi}{M} \right]}{\sin \left(\frac{\pi n}{M} \right)} \right| = \left| \frac{\sin \left(\frac{\pi n}{M} \right)}{\sin \left(\frac{\pi n}{M} \right)} \right|, \quad p^* \text{ is an integer} \quad (9)$$

It is approximately M for large M. This corresponds to the main lobe.

Let us now calculate $V_{p, k}$ for $k = k^* \pm 1$ to see the effect of the phase factor $e^{-j 2\pi Lkm/K}$ on the far grating lobes. From (5), we see that $V_{p, k^* \pm 1}$ is given by (7) with z replaced by $z \mp 1$. Thus,

$$|V_{p, k^* \pm 1}| = \left| \frac{\sin \pi LM(z \mp 1)/K}{\sin [\pi(Lz/K - p/M \mp L/K)]} \right| \quad (10)$$

Since $|z| < \frac{1}{2}$, $L < K$, the denominator of (9) can be appreciably larger than that of (7) depending on the choice of L, K, and M, while the numerators are about the same as that of (7). Specifically,

$$|V_{p^*, k^* \pm 1}| = \left| \frac{\sin (\pi n \mp \pi LM/K)}{\sin (\pi n/M \mp \pi L/K)} \right| \quad (11)$$

It is easily seen that $|V_{p^*, k^* \pm 1}| \ll |V_{p^*, k^*}|$. Thus the undesirable peaks at the immediate neighbor has been reduced. In general,

$$|V_{p^*, k^* + q}| = \left| \frac{\sin (\pi n - \pi q LM/K)}{\sin (\pi n/M - \pi q L/K)} \right| \quad (12)$$

Because of aliasing, we need to examine $|V_{p, k^* \pm 1}|$ for all p, not only for $p=p^*$. However, the overlapping of apertures of the first set of DFT's enables us to discard some of the $V_{p, k}$'s as illustrated in Figure 11.

Figure 11(a) shows the general problem posed by aliasing. Each K point DFT has the $\sin x/x$ response indicated and each filter processed in the second M-point

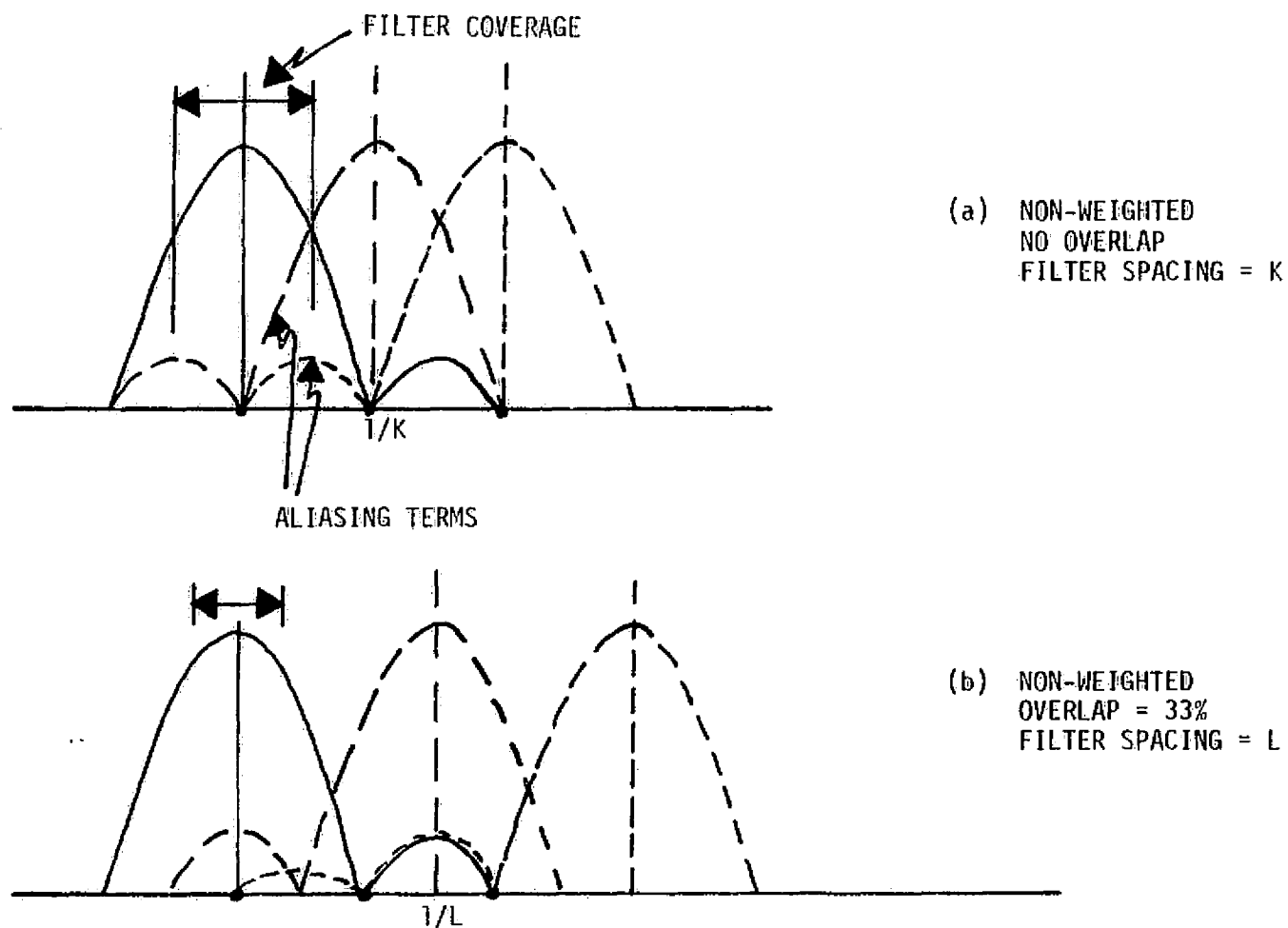


FIGURE 11. EFFECT OF OVERLAP ON ALIASING IN SECOND FFT RESPONSE

DFT produces M samples of high resolution within the filter response. However, aliased terms produced by sampling the spectrum at a rate proportional to $1/K$ fold back into the desired filter band from multiples of the sampling frequency.

If the sampling frequency is increased to $1/L$ (Figure 11(b)) the aliasing terms are reduced, but it is necessary to provide weighting to reduce them to acceptable levels. The combination of weighting factor, desired sidelobe level and sampling rate (overlap) can be balanced for a particular performance level.

Figure 12 shows the two dimensional frequency plane. The neighboring points along the first DFT direction, indexed by k , have a frequency separation of π/aK . The neighboring points along the second DFT direction, indexed by p , has a frequency separation of π/aLM . The frequency range covered by the M DFT coefficients along p is $M \cdot \pi/aLM = \pi/aL$ which is wider than π/aK . Thus we need only to retain $\frac{L}{K} \cdot M$ of these points, the others can be ignored.

The magnitude at the (p,k) point is $|Y_k V_{p,k}|$ where,

$$|Y_k| = \left| \frac{\sin(\pi\zeta)}{\sin[\pi(k^*-k+\zeta)/K]} \right| \quad (13)$$

and

$$|V_{p,k}| = \left| \frac{\sin\left\{\pi\left[n - \frac{LM}{K}(k^*-k)\right]\right\}}{\sin\left\{\pi\left[\frac{n}{M} - \frac{L}{K}(k^*-k) - \frac{p^*-p}{M}\right]\right\}} \right| \quad (14)$$

We note that $|Y_k| \approx K$ when $k=k^*$ and $|V_{p,k}| \approx M$ when $k=k^*$ and $p=p^*$, as expected.

From the previous discussion, it is clear we need to be concerned only with $|p-p^*| < \frac{LM}{2K}$ as indicated in Figure 13.

Since the overlap is equivalent to over-sampling, the grating lobe due to aliasing

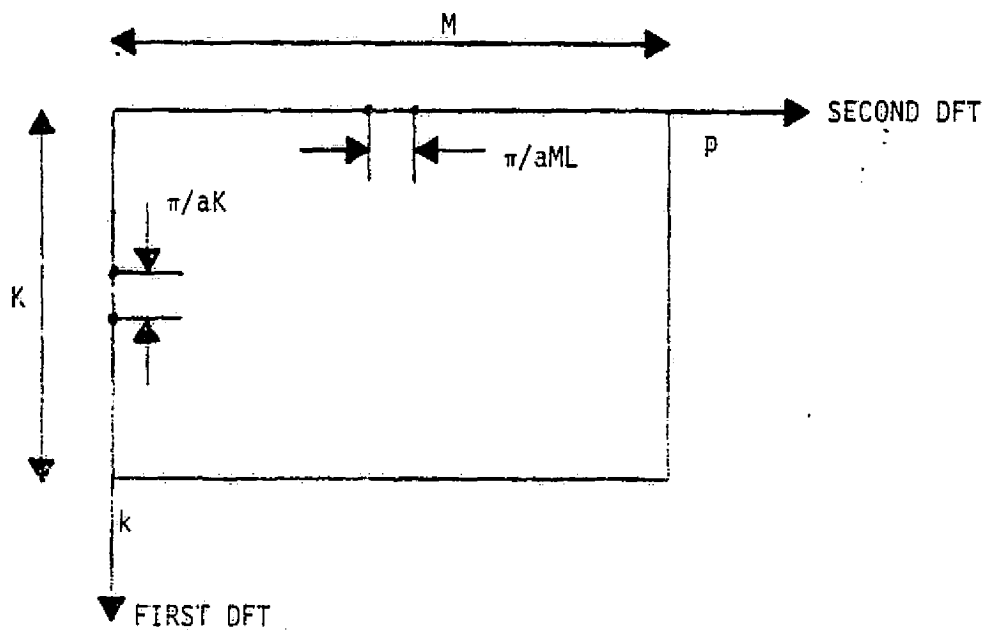


FIGURE 12. TWO DIMENSIONAL FREQUENCY PLANE

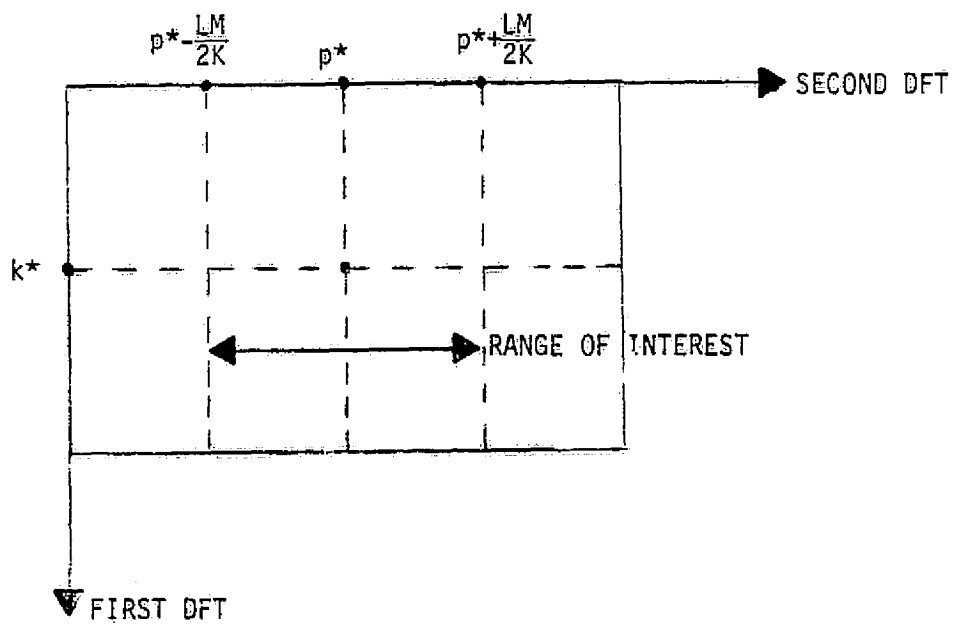


FIGURE 13. REGION OF INTEREST FOR OUTPUT POINTS

can be expected to be more noticeable when L is large. However, it is not obvious for what parameter values, the undesirable grating lobes will creep in to the range $|p-p^*| < \frac{LM}{2K}$. Values of $Y_{k,p,k}$ for some typical values have been computed.

Examples of the computed values are given in Tables 5a and 5b. The computer program permits selection of any system parameters and it can be used to search all sidelobes for problem areas for any set of processor parameters.

TABLE 5a. SAMPLE UNWEIGHTED RESPONSE CASE NO. 1

K	N	L	M	ML/K	P*	ETA				
8	64	5	12	4	1	0.50				
							0.936	0.162	0.097	0.077
										0.074
10	7	6	6	6	6	7	10	16		
0	0	-54	0	0	0	0	0	0		
9	9	10	11	15	24	72	-72	-24		
0	0	0	0	0	0	0	0	0		
-98	-128	-203	-597	597	203	128	98	84		
0	0	0	0	0	0	0	0	161		
-61	61	21	13	10	8	8	8	8		
0	0	0	0	0	77	0	0	0		
10	7	6	6	6	6	7	10	16		

TABLE 5b. SAMPLE UNWEIGHTED RESPONSE CASE NO. 2

K	N	L	M	ML/K	P*	ETA				
8	64	3	19	4	2	0.50				
							0.812	0.220	0.140	0.115
										0.10
0	0	0	0	0	0	0	0	0		
3	3	4	5	8	19	-126	-14	-7		
33	19	13	10	9	8	7	7	6		
-21	-21	-21	-22	-24	-26	-31	-38	-51		
-78	-106	-174	-517	517	174	106	78	63		
-19	-15	-13	-12	-11	-10	-10	-10	-11		
5	5	6	6	8	10	14	25	125		
-12	-112	16	7	5	3	3	2	2		
0	0	0	0	0	0	0	0	0		

2.2.5 Summary of Step Transform Processing Factors

The important factors which have to be considered in order to minimize sidelobe level are: (see Figures 14 and 15)

1. Input spectral aliasing.
2. Sidelobes of the spectral coefficients (short aperture).
3. Time sample aliasing of first FFT coefficients.
4. Quadratic phase change from step to step.
5. Straddling loss due to time sampling.
6. Second FFT sidelobes.
7. Amplitude variations due to coefficient amplitude versus frequency characteristic in both the first and second FFTs.

The first item above involves the time sampling of the range compressed input baseband signal. Since the sampling is complex this should be at least equal to the bandwidth of the signal. Since there is no perfect band limiting filter, a guard band is necessary to avoid spectral foldover losses. Sampling rates of the order of 1.1 to 1.5 times Nyquist will provide low sampling losses due to aliasing (depending upon the bandlimiting filter characteristics). The output of the first spectrum analyzer will include the full coverage of the spectrum up to the sampling frequency. Those coefficients outside the bandwidth of the signal can be dropped before going into the storage memory.

A very important factor which must be included in order to minimize the system sidelobe levels is that time weighting must be applied across the aperture of the first FFT. If time weighting were not applied each Fourier coefficient would have a $\sin x/x$ sidelobe response which would result in unacceptable sidelobes for most radar signal processing. Weighting will increase the main frequency lobe width for each coefficient, and lower the sidelobes according to the weighting

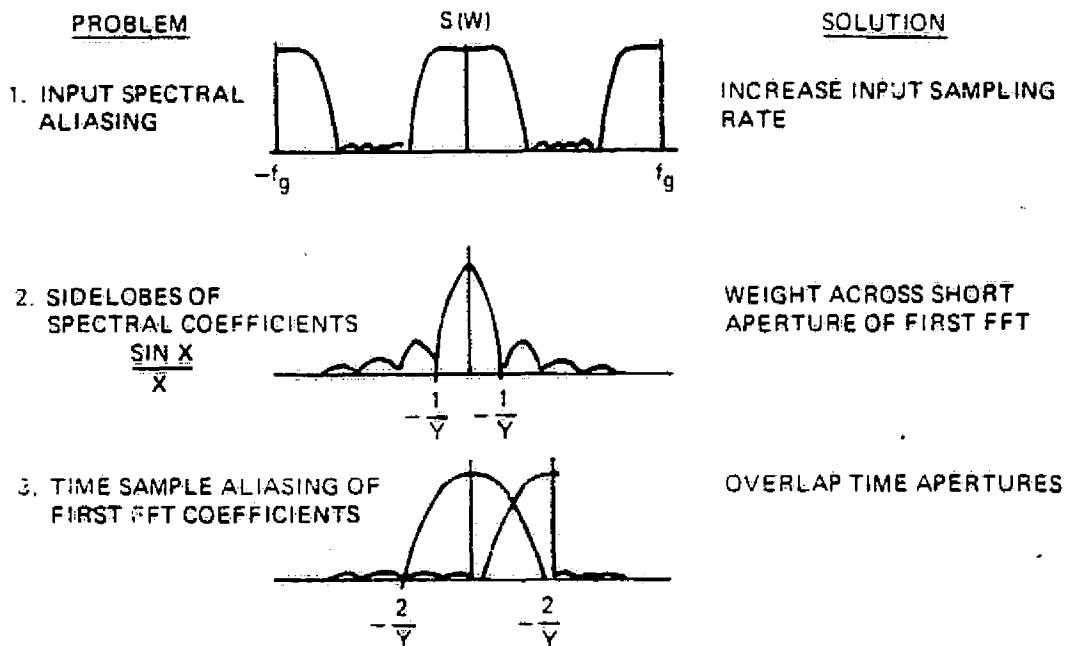


FIGURE 14. PRACTICAL IMPLEMENTATION OF STEP TRANSFORM MATCHED FILTER

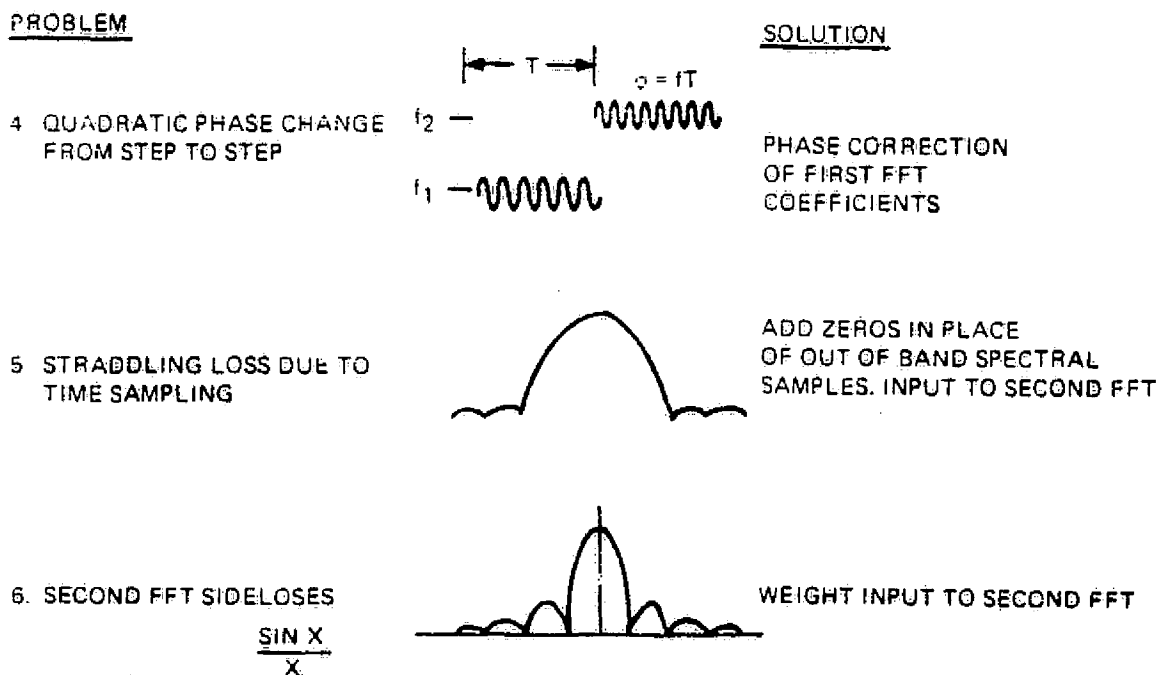


FIGURE 15. PRACTICAL IMPLEMENTATION OF STEP TRANSFORM MATCHED FILTER (CONTINUED)

function used.

The second FFT receives sequential samples derived from adjacent subarrays of the first FFT. The sampling rate from the first FFT output must be sufficient to prevent aliasing in the second FFT. To increase the sampling rate out of the first FFT it is necessary to overlap the subarray apertures. Since the weighting function across the subarrays widens the bandwidth covered by each spectral coefficient there is a large amount of overlap in frequency. Not all frequencies covered by a coefficient from the first FFT are extracted from that coefficient. Therefore, some time sampling aliasing can be tolerated provided it does not cause aliased signals to fall in the frequency region where the fine resolution frequencies are to be extracted. The useful region for a low resolution coefficient is equal to the frequency difference between coefficients or the reciprocal of the aperture of the first FFT.

Another factor which must be applied is a quadratic phase correction to the input of the second FFT to remove the effect of simultaneously stepping in time and frequency. The mathematical analysis of the previous section has shown why this factor exists and the deterministic correction required.

The output sampling rate of the matched filter should be higher than that of Nyquist sampling to minimize the effects of straddling loss. The sampling rate can be increased without changing the clock rate since the Fourier coefficients of the first FFT which represent the "guard band" and have been discarded can be replaced by "zeros" in the second FFT. This will increase the output sampling rate without changing the output waveform shape or bandwidth.

Close-in sidelobes which result from the second FFT operation can be reduced by amplitude weighting on the input to that FFT. This will reduce the sidelobes according to the weighting function selected.

Since the data is being continuously fed into the step transform process, the overlapped subarray computation can be performed as a running process. Similarly, the output fine resolution can be computed as soon as a full aperture of subarrays have been computed. This is also done as a running process where new subarray data is added while the old data is dropped. The second FFT weighting function is time shifted corresponding to the beginning of the overlapped subarray data. This will provide a stepped sliding aperture weighting which will minimize sidelobe effects of large point scatterers.

2.3 BASELINE PROCESSOR DESIGN STUDY RESULTS

2.3.1 Baseline SAR System Design

2.3.1.1 System Parameter Definition - The baseline SAR azimuth processing system requirements are represented diagrammatically in Figure 16. As the satellite maps an image field, four separate looks are generated for each image sample. Each look consists of 1024 azimuth samples which cover a 100 km range swath. Four looks require a total of 4096 azimuth samples. One fourth of the total of 1024 (or 256) azimuth elements complete the four-look integration during a look. Thus the basic word data rate from the input to the output of the processor is reduced by a factor of four.

The basic requirement of the SAR azimuth processor is to process the 1024 azimuth samples which represent 1024 spatial element samples of a synthetic array into an equal number of azimuth angle elements (beams) for each range element in the 100 km swath. The process is complicated by the fact that during the four-look interval, a particular image element will walk, or migrate, in range as indicated in Figure 17. The range migration is such that the maximum migration during the four looks is 128 range elements and about one fourth of this total during a single look.

The range migration has been assumed to be identical for each range in a given azimuth beam although variation can be accommodated in the implementation to be discussed later.

Key processing parameters for the baseline SAR system are given in Table 6.

The objective of the subarray approach is to subdivide the SAR processing in a manner which permits range migration compensation to be applied on a subarray resolution basis rather than for each individual azimuth and range sample. This will also minimize any signal to noise loss and smearing that results during the subarray integration.

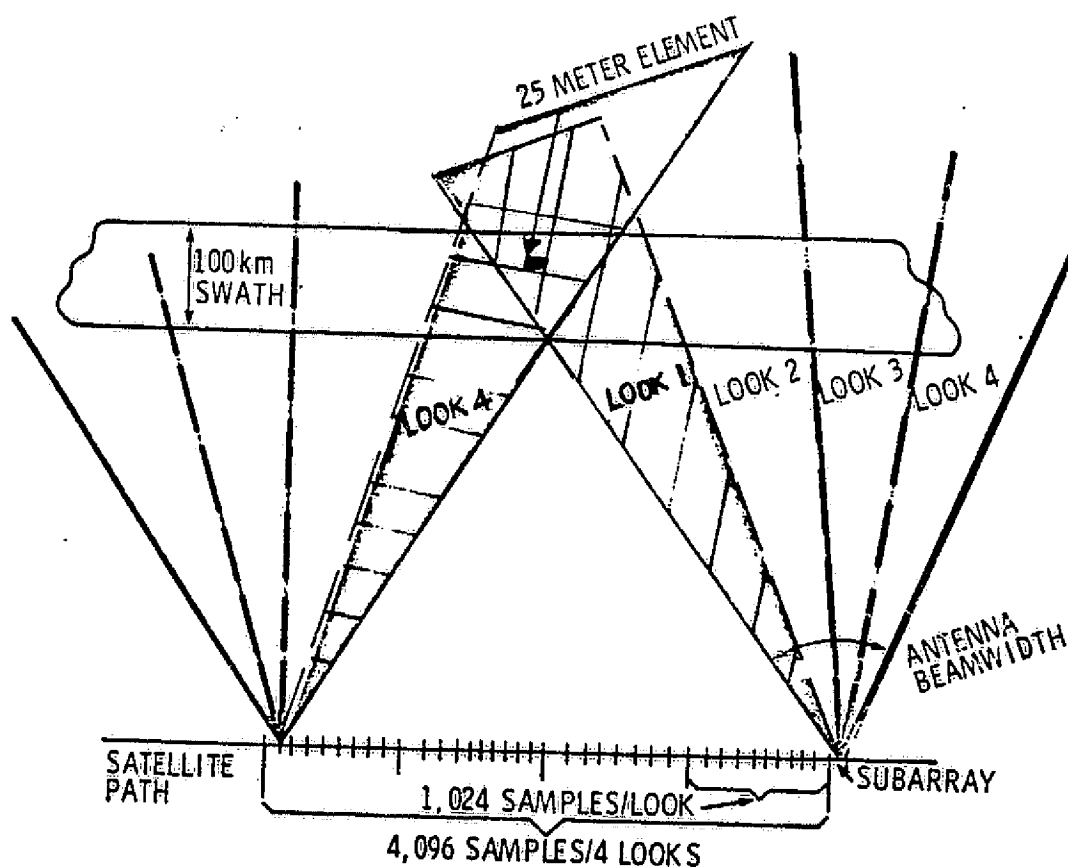


FIGURE 16. BASELINE SAR SYSTEM PARAMETERS

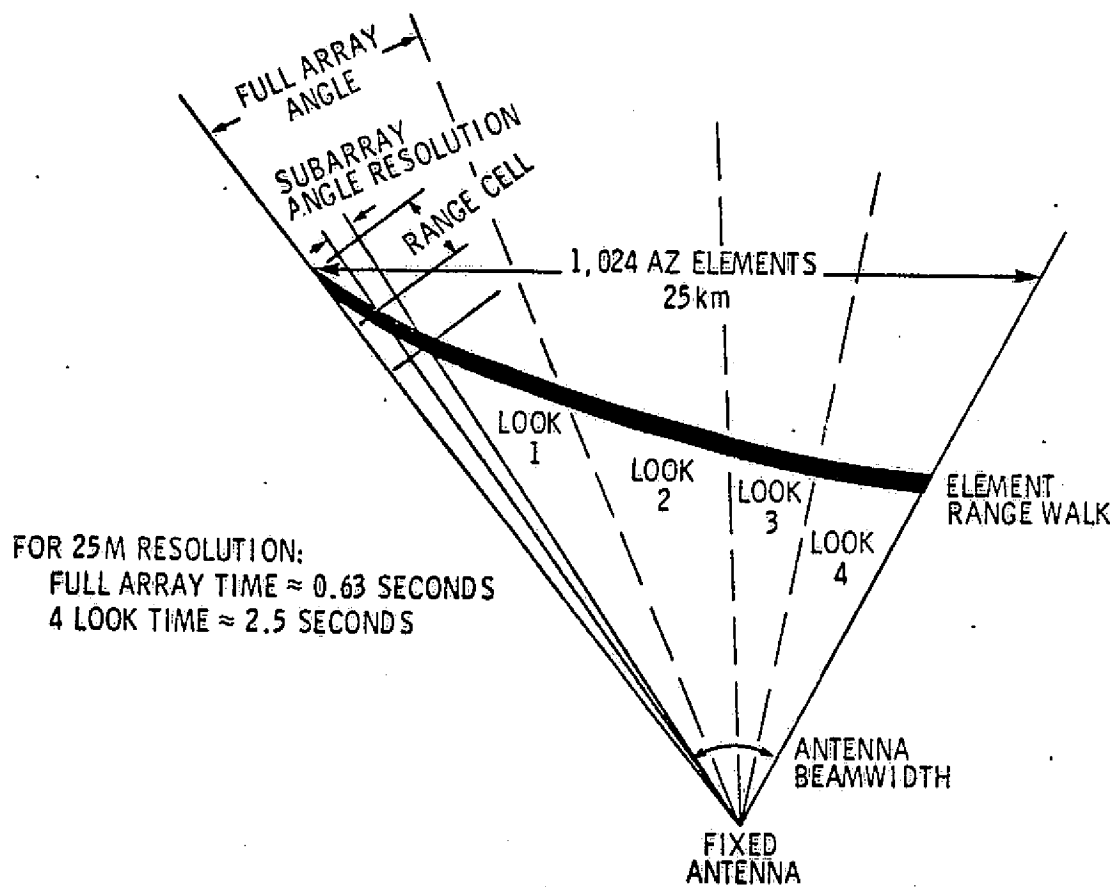


FIGURE 17. RESOLUTION ELEMENT MOTION
 RELATIVE TO FIXED ANTENNA

TABLE 6. BASELINE SAR PROCESSING PARAMETERS

SWATH WIDTH: 100 km	RANGE SAMPLES: 1152
RESOLUTION: 25 m	RANGE MIGRATION: 128 RANGE
PRF: 1645 Hz	ELEMENTS
NUMBER OF LOOKS: 4	(4 LOOKS)
AZIMUTH SAMPLES PER LOOK: 1020	INPUT QUANTIZATION: 6 BITS
	I AND Q

The maximum subarray size is determined by the range walk, which is acceptable during a subarray integration time. The general equation for range walk is,

$$\Delta R = \int_0^T \dot{R}(t) dt$$

For $\dot{R}_0 < 353$ meters/sec (based on 1° roll, pitch and yaw) and $\ddot{R} \approx 59.4$ meters/second² (relative motion of earth to satellite),

Assuming that an allowable range walk of one half a resolution cell provides acceptable system performance, the time limit to keep the range migration within one half of a radial range resolution cell of 8.34 meters is .0083 seconds. This gives a maximum of 14 pulses per subarray. In addition the equation can be used to determine the range migration across four looks (2.5 seconds) of 128 range elements and across the worst case look (0.63 seconds) of 36 range elements.

Fourteen azimuth samples per subarray is small for efficient application of the step transform subarray process. In order to increase the maximum subarray size a linear range walk correction can be applied prior to subarray processing. The average range rate is 427 meters per second. If this is applied initially the maximum remaining differential range rate is 75 meters/second. The maximum subarray integration time is then .056 seconds or 92 pulses to keep the range walk within one half of a range resolution element.

Another factor of concern is the rotational range walk between subarrays illustrated

which can also provide some smearing of the range resolution cells and effect both signal to noise output and ultimate angular resolution.

The rotational range walk effects are shown in Figure 18. For a radar antenna beamwidth of 1.28 degrees the single look rotation angle is 0.32 degrees.

For a rotational range walk of less than ± 0.5 range cells (8.34 meters) the corresponding subarray resolution must be no greater than $8.34/\sin(0.32^\circ) = 1494$ meters. Therefore, the minimum subarray size (for this maximum resolution) is,

$$\frac{25}{1494} \times 1020 = 17 \text{ samples}$$

The number of subarrays selected for the baseline SAR processor is 64 which gives 16 subarrays in the 1024 azimuth sample aperture. However, in order to avoid spectral aliasing it is necessary to overlap subarrays in the step transform process. The minimum number of subarrays per aperture is then about 36 for -40 dB pattern sidelobes.

One final problem is multilook registration shown in Figure 19. In order to place the multiple look grids in registration it is necessary to range interpolate each subarray beam. The grids are lined up in azimuth by frequency shifting each range bin prior to the final subarray combination. For a 64 pulse subarray the maximum registration error within a subarray is then 0.41 range elements. A separate frequency must be applied for each look to correct for multilook bias errors.

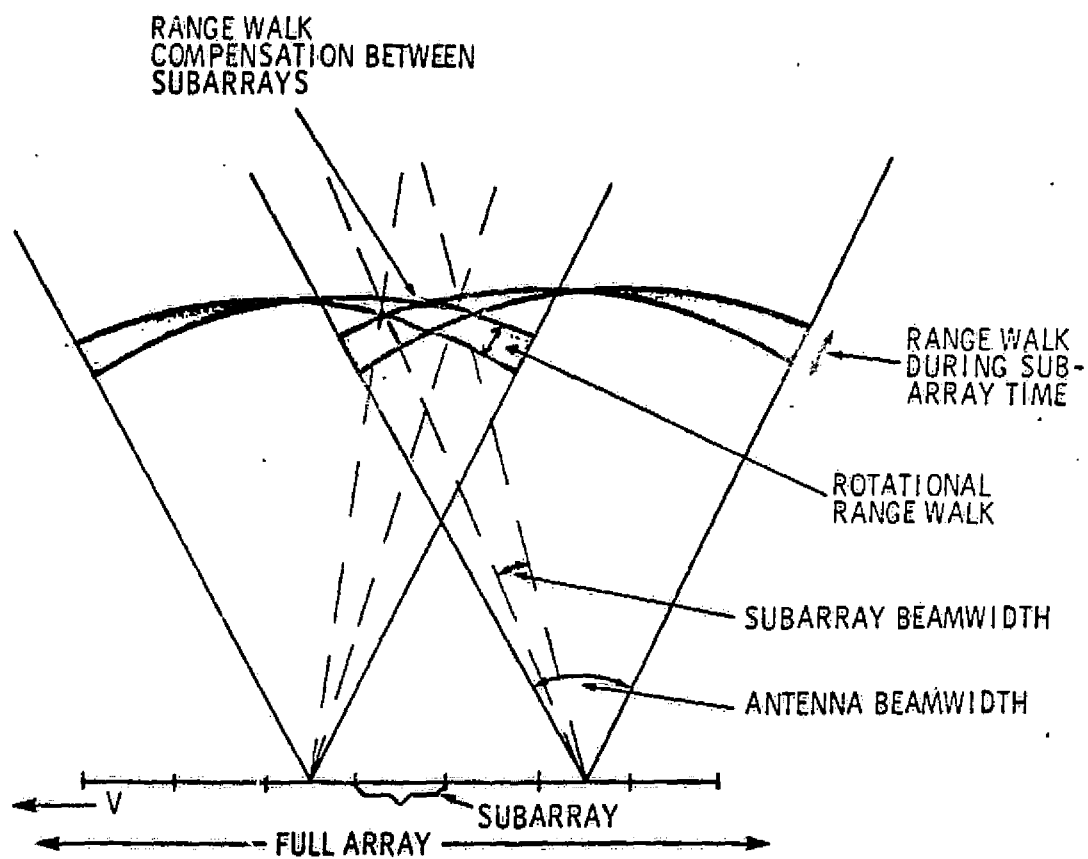
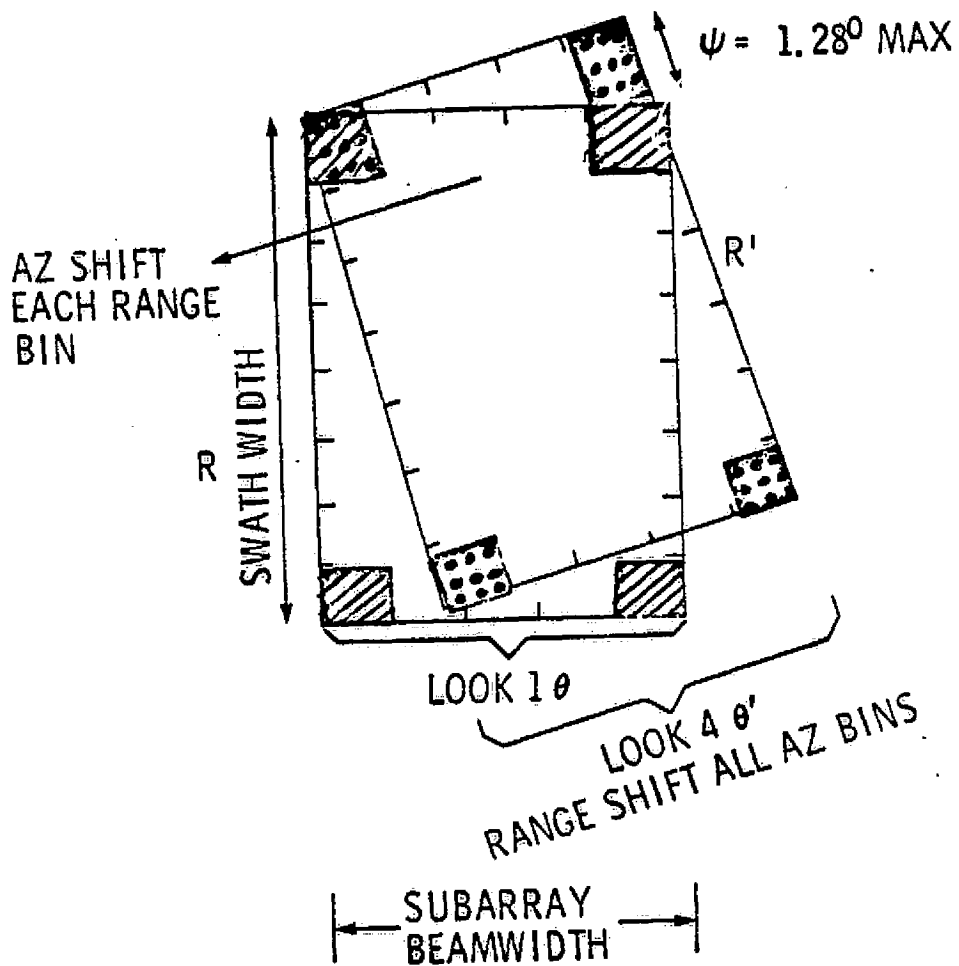


FIGURE 18. ROTATIONAL RANGE WALK BETWEEN SUBARRAYS

GRID CENTERED IN RANGE
AND AZIMUTH FOR EACH
SUBARRAY BEAM BY RANGE
INTERPOLATION AND AZIMUTH
FOCUSING FUNCTION.



ROTATION: $\theta' = \theta \cos \psi - R \sin \psi \approx \theta - R \sin \psi$
 $R' = \theta \sin \psi + R \cos \psi \approx R$
 FOR 64 PULSE SUBARRAY: $\theta = 305$ METERS
 MAX ERROR: $R' = \theta \sin \psi = 305 \sin 1.28^\circ$
 $= \pm 0.41$ RANGE BINS

FIGURE 19. MULTILOOK REGISTRATION

2.3.1.2 Performance Level of Baseline System - Since the step transform subarray processor adjusts for range walk effects from subarray to subarray, there are residual range walk effects at the edges of the subarray beams which are not compensated. These uncompensated range walk effects are shown in Figure 20. Although the average range rate is subtracted by the analog to digital converter timing, each azimuth element will move according to its velocity relative to the antenna during the subarray integration time. There is little range walk variation in subarray beams perpendicular to the line of flight. However, subarray beam positions near the edge of the real antenna beam will have the largest range walk. Additional uncompensated range walk effects occur due to misregistration rotation of the images in each subarray output when they are combined with the other subarrays. The worst misregistration effects also occur at the edges of the real antenna beam.

The effect of the uncompensated range walk when performing azimuth focusing integration is to "smear" the range resolution cell. This results in reduced range resolution in the range direction and loss of signal to noise ratio. The effect on the output azimuth elements will be some changes in sidelobe structure, limited azimuth smearing and some bias displacement. The extreme effect, of course, is when the image element has moved completely out of the range resolution cell and no further azimuth integration can be accomplished.

The uncompensated range rate during the subarray is defined as the actual range rate minus the average range rate or:

$$\text{Uncompensated Range Rate} = \ddot{R} \left(t - \frac{T_{\max}}{2} \right)$$

The rotational range walk between subarrays can be determined by:

$$\text{Rotational Range Walk} = \frac{L}{2} \sin \theta$$

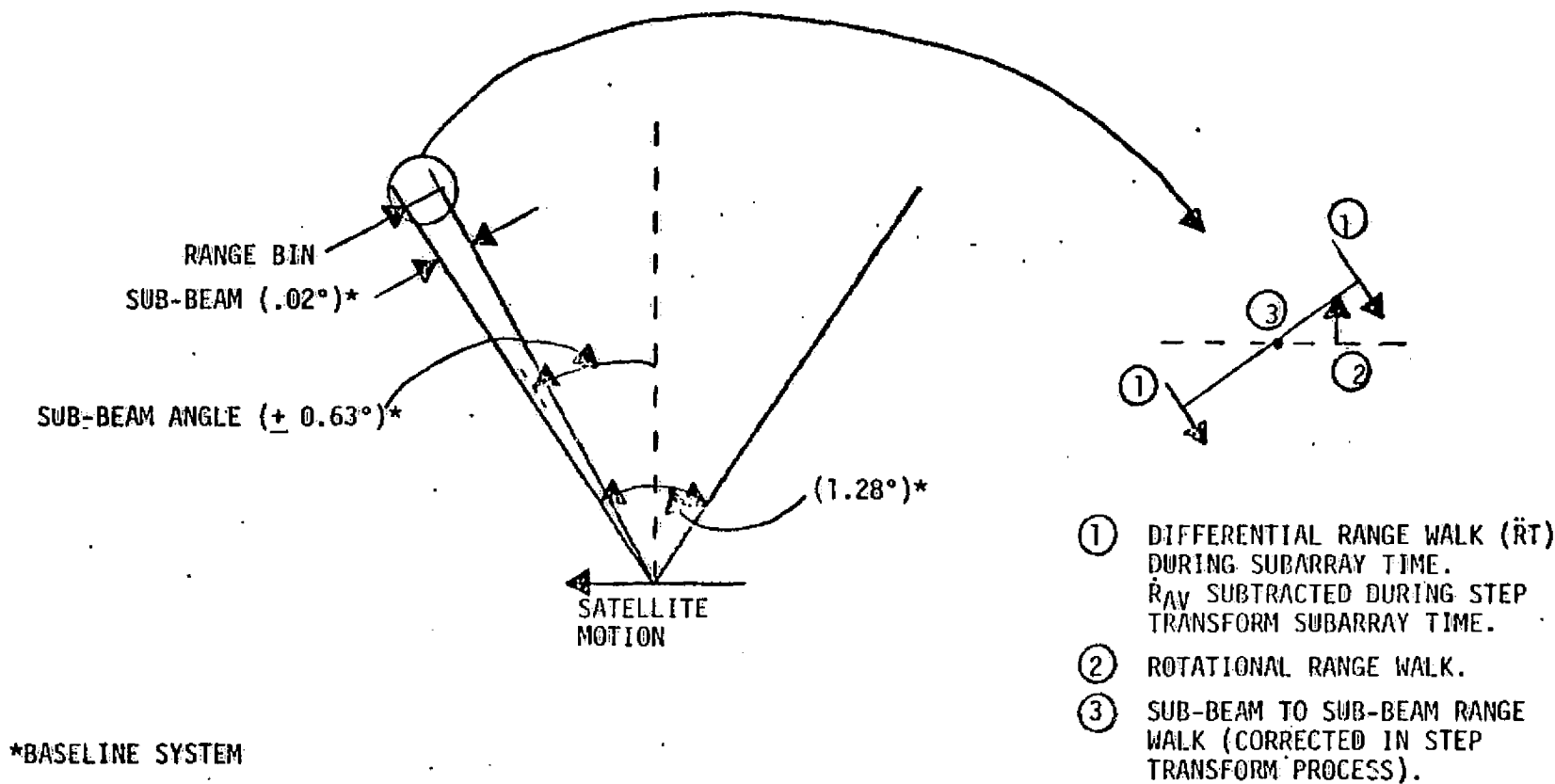


FIGURE 20. UNCOMPENSATED RANGE WALK EFFECTS

where L is the azimuth sub-beam ground width and θ is the antenna beamwidth.

The effect of range walk on smearing the range resolution cell can be calculated by approximating a single pulse range cell as a Gaussian function normalized to unity and displacing its mean by the range walk.

Then,

$$\text{Radar Return Pulse} = Ae^{-0.347(x-R_w)^2}$$

where R_w equals range walk (normalized to unity range resolution cell) which equals rotational range walk plus differential range walk.

For the baseline system, integrated range resolution equals:

$$\sum_{K=1}^{K=4096} Ae^{-0.347(x-R_{wK})^2} = \sum_{h=1}^{64} \sum_{K=1}^{64} Ae^{-0.347(x-R_r(n)-R_D(K))^2}$$

where,

$$R_r(n) = 18.29 \sin \theta_n$$

$$\theta_n = (n-1)(.02) + .63$$

$$R_D(K) = \frac{K}{64} (.0108n + .3526)$$

Performing the summation for both the baseline system and a maximum specification system where $R_D = 0.5$ and $R_r = \pm 0.5$ range bins results in the following increases in range resolution cell size and loss in signal to noise ratio.

	INCREASE IN RANGE RESOLUTION CELL	LOSS IN SIGNAL/NOISE
BASELINE SYSTEM	.02	0.15 dB
MAX. SPEC. SYSTEM ($R_D = 0.5$, $R_r = 0.5$)	.06	0.56 dB

Figure 21 shows a plot of the integrated range cell for the baseline system as compared to the single return Gaussian pulse.

Figure 22 shows the same thing for the maximum specification system.

These results show that the range smearing cell size is negligible when the maximum range walk deviation is kept to less than half a range cell.

It is expected that similar results will be obtained in the azimuth resolution effects although these simulations were not performed as part of this study effort.

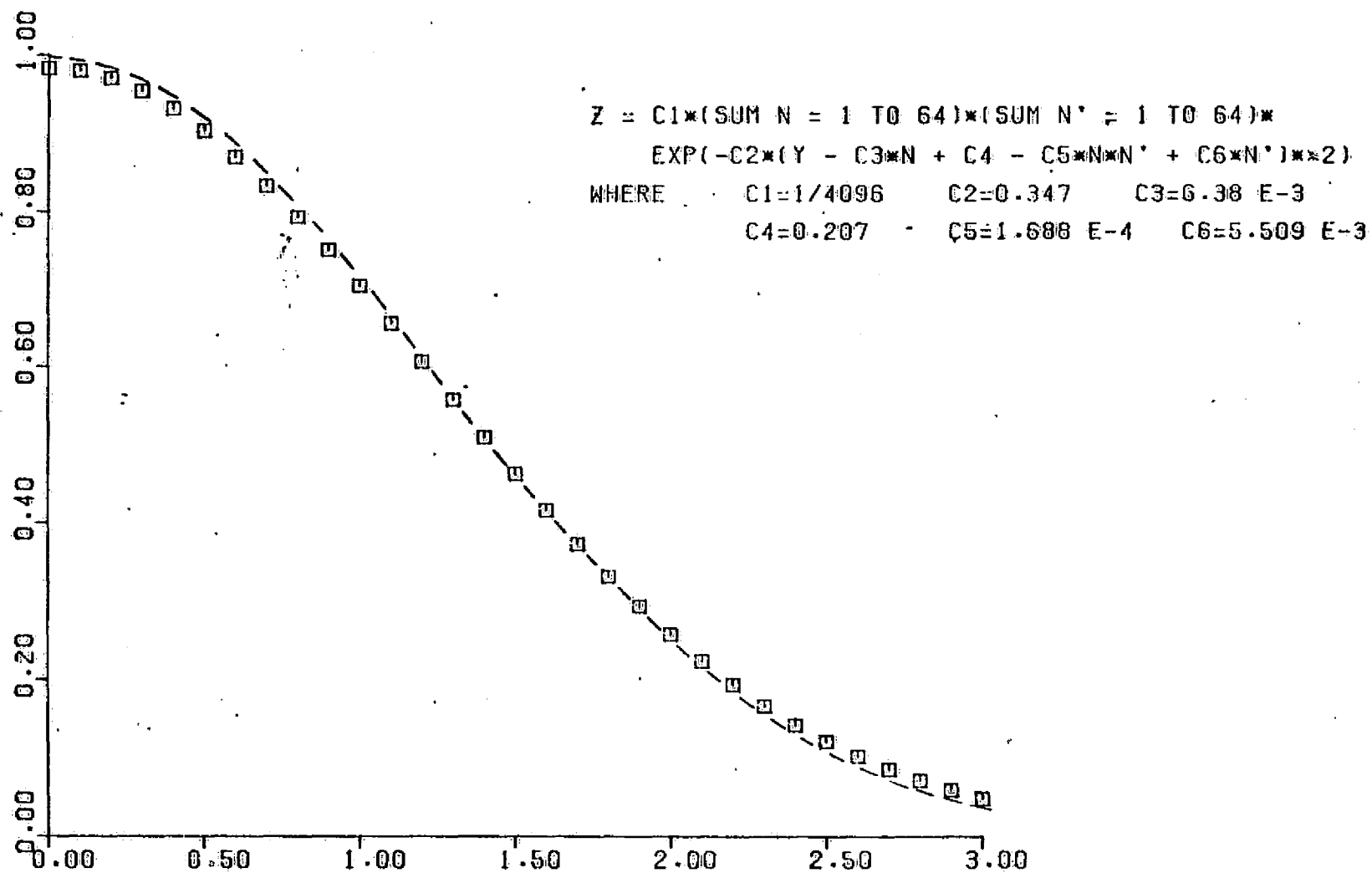


FIGURE 21. INTEGRATED RANGE CELL FOR BASELINE SYSTEM (COMPARED TO IDEAL GAUSSIAN)

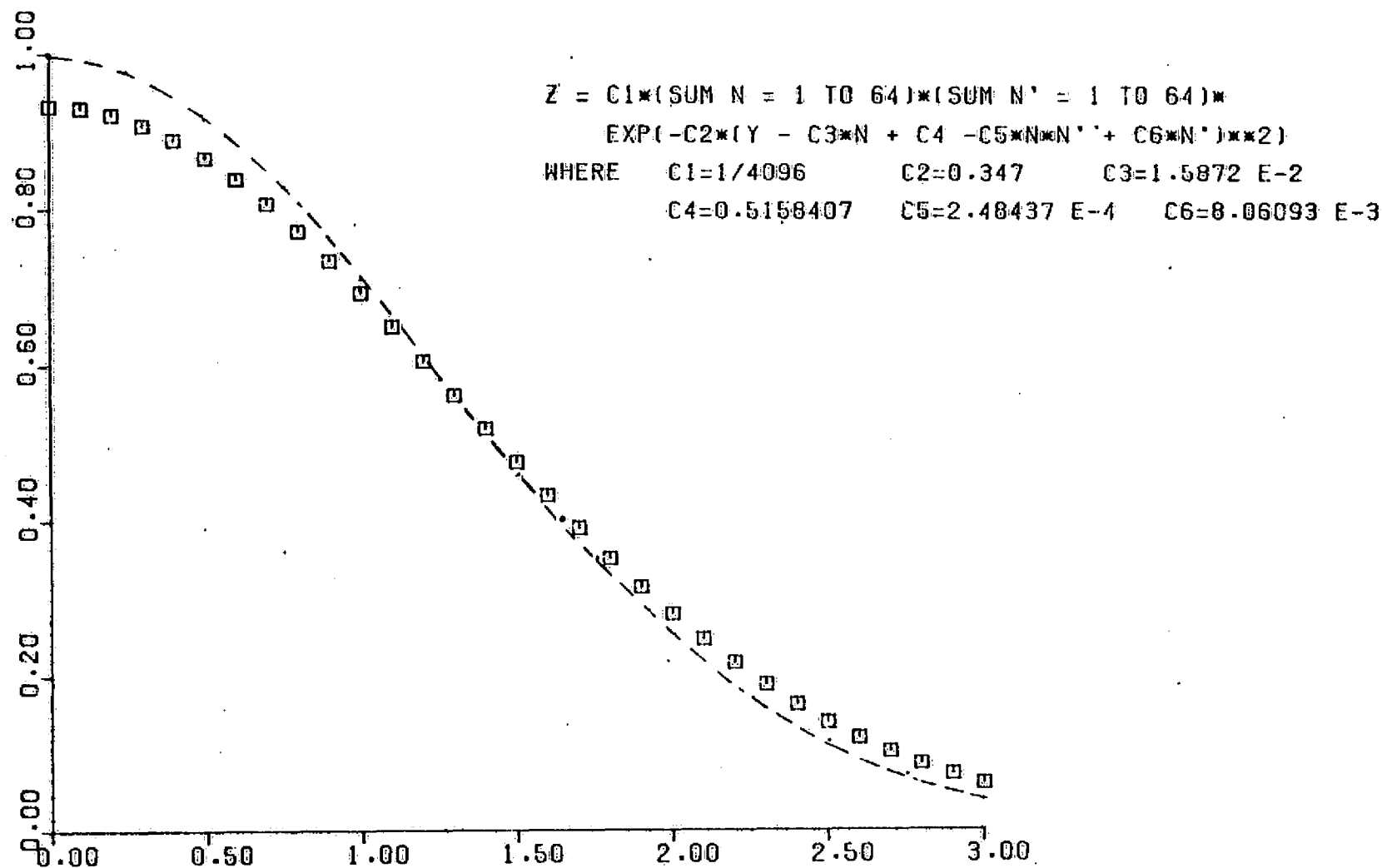


FIGURE 22. INTEGRATED RANGE CELL FOR MAX. $R_D = 0.5$, MAX. $R_r = 0.5$ (COMPARED TO IDEAL GAUSSIAN)

2.3.2 Implementation of Baseline System

2.3.2.1 Baseline SAR Processor Design - A general block diagram of the baseline processor is shown in Figure 23. A linear range walk correction is applied at the A/D converter. The corner turning memory changes the order of the data from range to azimuth samples. After subarray beam formation range walk correction is applied. Multilook rotation correction is incorporated in the subarray combination function. The multiple looks are integrated and stored in an output memory.

Details of the implementation of the step transform processor shown in Figure 24 apply the general step transform processor architecture to the specific system requirements of the baseline SAR system. Range compressed data is received by the azimuth processor and assuming the range compression is done at an IF frequency, the sample data must pass through a PRF buffer to minimize the computational rate requirement of the processor.

The baseline implementation places the corner turning memory immediately after the PRF buffer. A batch processor is formed with this configuration which greatly simplifies the corner turning memory. The price paid is a loss in efficiency of the antenna beam. The beam must illuminate about 25% more area. This is necessary to assure that each azimuth sample employed in integrating over four looks has received energy from all image points. An alternative approach is to implement a continuous strip map processor which uses a minimum antenna beamwidth. The implementation of the continuous strip map processor, however, results in a complication of the memory systems. This is discussed in further detail in Section 2.4.2.2.

Data is read from the corner turning memory on a range slice basis with the azimuth

samples in natural pulse order. Subarrays are next formed in the overlap buffer which simultaneously forms the overlapped subarrays and places the data in a radix-2 (two parallel complex data channels) format for processing in the pipeline FFT. With an overlap factor of 2.28 and an input data rate of 1.9 MHz the output data rate to the FFT is 2.2 MHz.

The linear FM phase function is deramped prior to entry to the FFT and the result for a given range element is a set of 36 CW segments each of 64 samples in length and overlapped by 36 samples. The spectrum of these segments is then received by the coarse range migration memory where the data is stored in a range-beam format. Each subarray has 64 beam positions and conversely each beam has 36 subarrays.

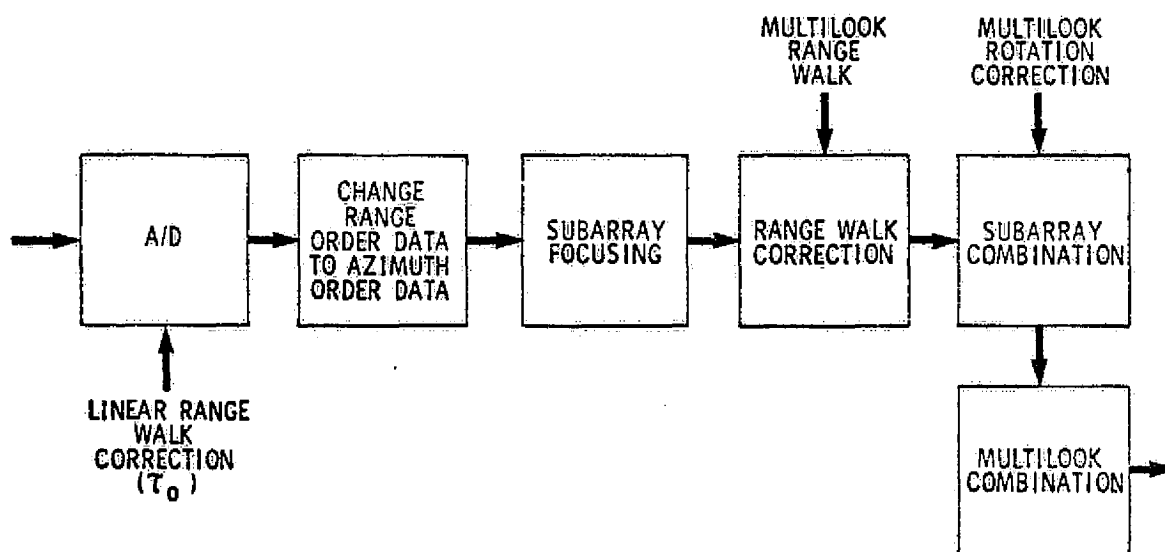


FIGURE 23. BLOCK DIAGRAM OF AZIMUTH PROCESSING FUNCTIONS

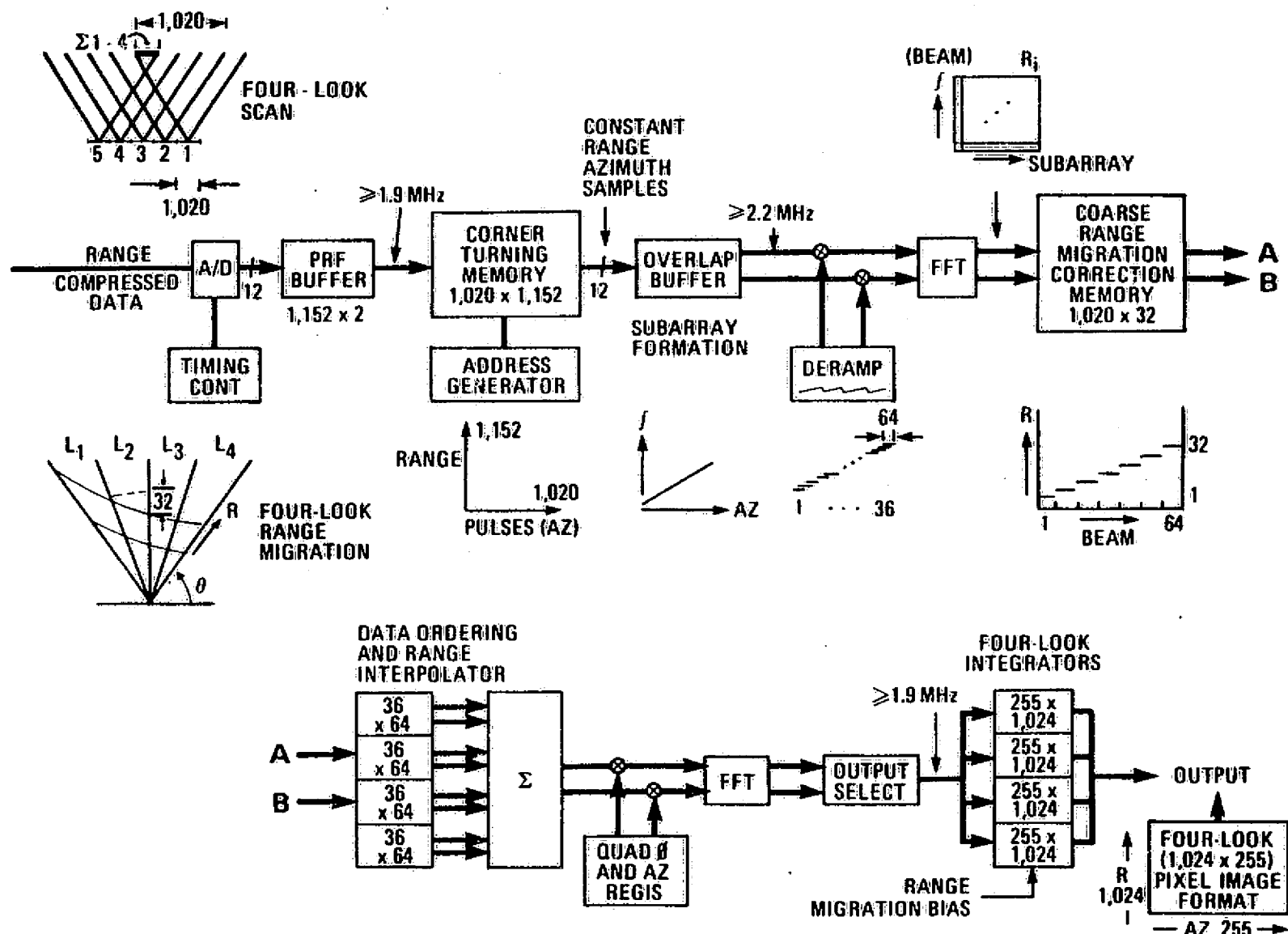


FIGURE 24. IMPLEMENTATION OF STEP TRANSFORM SUBARRAY SAR PROCESSOR 20 km SWATH

Data is read from the coarse range migration memory on a true range basis across all 64 beams with 36 subarray samples per beam. Each constant range line thus formed is placed in a data reordering memory of $36 \times 64 = 2304$ word capacity. Four such memories are paralleled to form four adjacent range element sets. Data is read from all four memories simultaneously to provide an interpolated range sample. A fifth data reordering memory is required to provide continuous operation. Data is read from the reorder memory for all beam positions along a beam-subarray diagonal. Details of the data conditioning for entry to the second FFT remain to be developed. Quadrature phase and azimuth registration correction is applied prior to entry to the second FFT. The data at the output of the second FFT is in the time domain and the desired output samples must be selected and ordered to provide a natural beam ordered output.

The final outputs are integrated in the four look integrating memory as magnitude samples. A 1024 range cell by 255 azimuth cell image map is completed during each look interval. The final output data rate is thus one fourth of the input rate.

2.3.2.2 Semiconductor and Memory Technology - The power dissipation of a digital system is essentially determined by the power-delay product of the technology employed assuming an efficient design. Several current semiconductor technologies with low power-delay product are compared in Figure 25. The figure shows that current and projected CMOS/SOS* technology provides an optimum technology choice for LSI and VLSI systems. The shaded portion of the graph indicates the expected performance of CMOS/SOS as narrower channel lengths are employed. Current technology uses 6 micron channels and as electron beam

* Complementary metal oxide semiconductor, silicon on sapphire substrate.

lithography techniques are perfected channel lengths to 4, 2 and 1 micron can be expected.

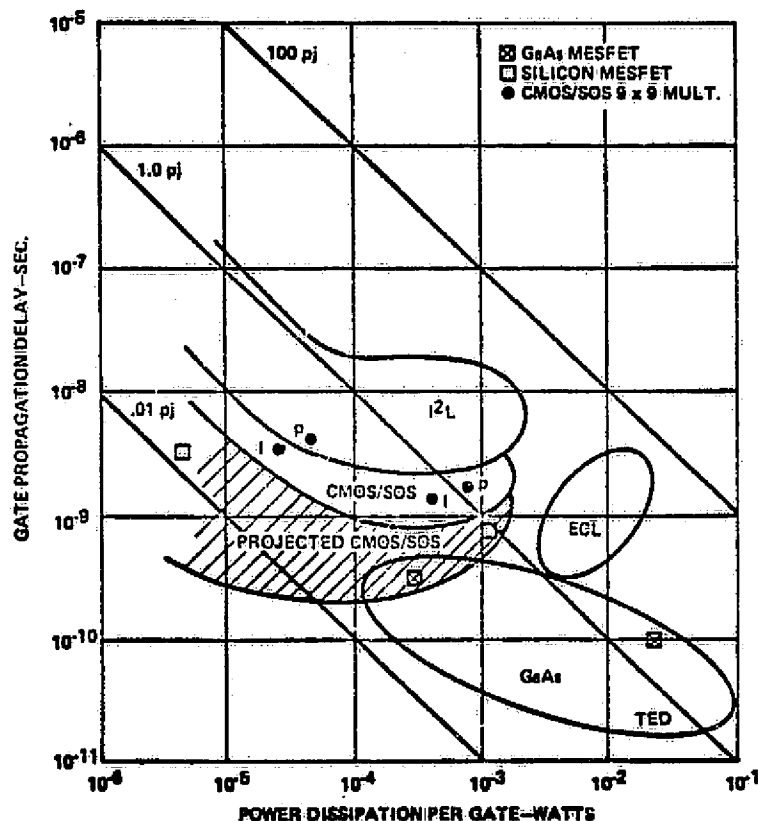


FIGURE 25. POWER DELAY PRODUCT COMPARISONS

The primary hardware constituent of the SAR signal processor will be memory. Thus for ultimate low power, size and cost semiconductor memories of maximum capacity are required. Figure 26 shows the general trend versus time of semiconductor memories. Based on this curve and the realities of today's commercial market, indicated by the vertical line at the mid-1978 point, one can expect to have 64K RAM's available for an on-board SAR processor in the mid-1980's. This is supported by the fact that five companies (Hippon, TI,

Fujitsu, Motorola and National) have announced production plans for 64K units for late 1978. IBM is currently using 64K RAM's in its 8100 series computers.

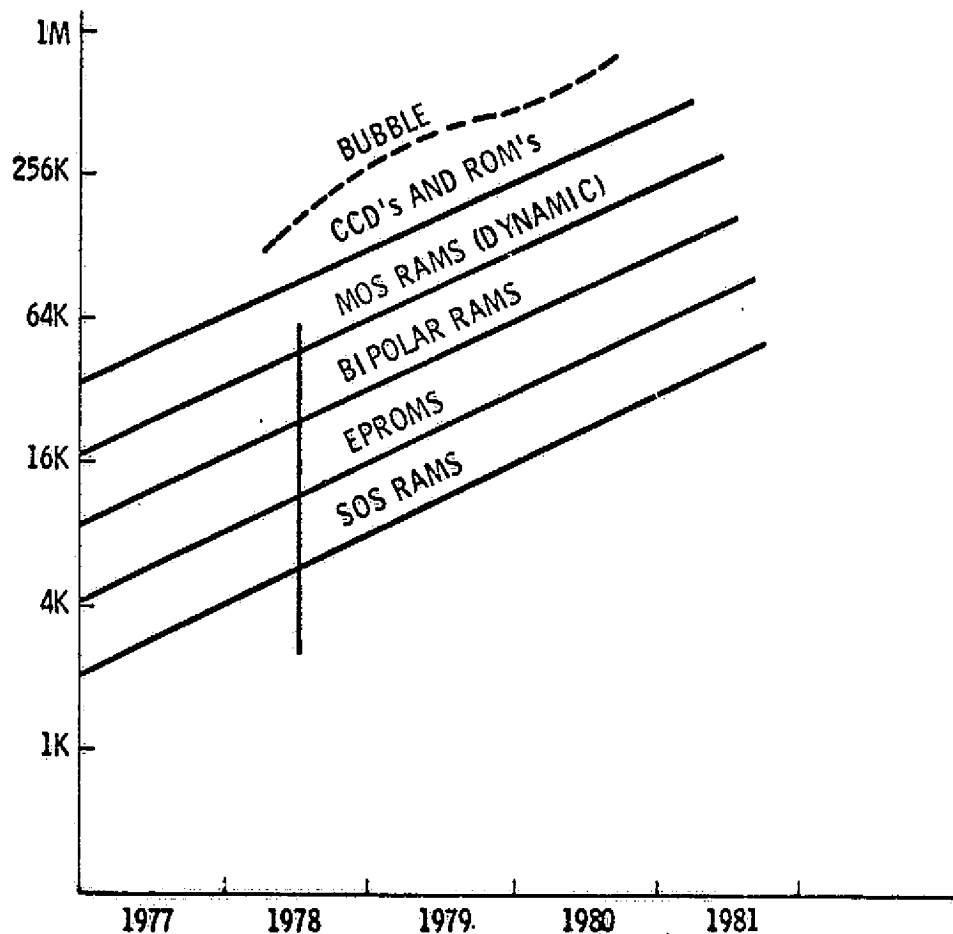
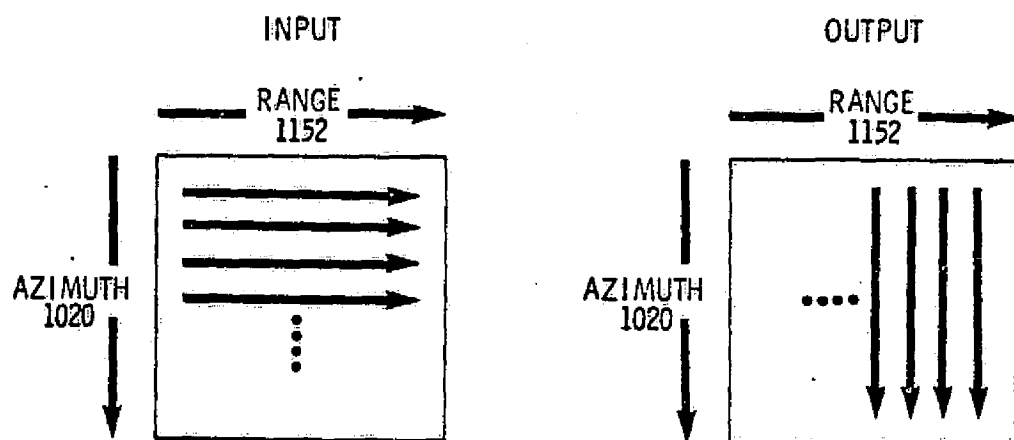


FIGURE 26. MEMORY CHIP CAPACITY TRENDS

2.3.2.3 Memory Implementation - A key memory element is the corner turning memory whose requirements are indicated in Figure 27. This memory can most simply be implemented as a large, double buffer but in the particular application the sheer size of the memory storage (14×10^6 bits) negates this approach. RCA has developed an addressing algorithm for the corner turning memory application which permits the corner turning function to be implemented

with a single memory as shown in Figure 28. The memory, however, must be somewhat faster than if the double buffer approach is used since a full read and write cycle must take place in the sample time of 525 nsec (corresponding to the I/O rate of 1.9 MHz).



- CAPACITY: SINGLE MEMORY = 14.2×10^6 BITS
- INPUT, OUTPUT RATE = 1.9 MHz
- FOR SINGLE MEMORY
 - READ/WRITE CYCLE = 525 nsec
 - ACCESS TIME = 200-250 nsec

FIGURE 27. CORNER TURNING MEMORY

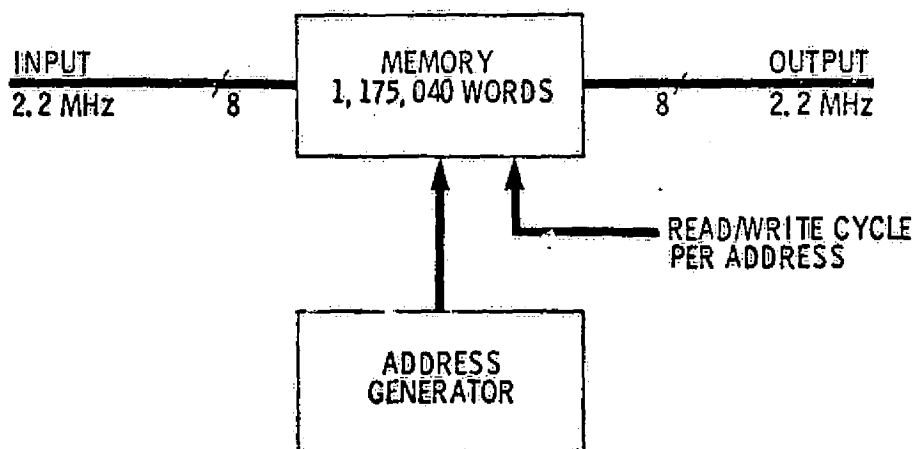


FIGURE 28. SINGLE MEMORY CORNER TURNING

Subarray formation is accomplished in the manner shown in Figure 29. Data at the input rate of 1.9 MHz is fed alternately to each of three multiplexed memory units. A new memory unit load cycle is begun every 28 input sample periods. In loading the memories, the first 32 words are loaded into one half and the second 32 words are loaded into the second half. Thus, when the data is read out simultaneously on two parallel lines for radix-2 operation, a factor of two reductions in speed is obtained. With the given parameters, the net clock rate at the output becomes,

$$\frac{64}{28} \times \frac{1}{2} \times 1.9 \text{ MHz} = 2.2 \text{ MHz}.$$

The total memory requirements for a 20 km swath, excluding memories within the FFT's, is shown in Table 7. Two separate totals are developed, one of which uses 16K memory circuits and the second for 65K memories.

The memory power dissipation can be estimated to settle anywhere from one to six microwatts per memory bit. Current static MOS memories such as the Intel 2141L 4K x 1 RAM have an internal power down feature which can reduce the average power dissipation up to 90 percent. The Intel circuit consumes 25 mW or 6 μ W per bit in the powered down mode. CMOS/SOS RAM's on the market consume about 1 μ W per bit. Examples of these are two RCA 4K RAMs, the MWS 5114 and the CDP 1825. The total bulk memory in the 20 km swath SAR baseline processor is about 25×10^6 bits. This projects to memory power dissipation of 25 to 150 watts based on the 1 μ W to 6 μ W per bit rule.

2.3.2.4 Pipeline FFT's - Two transform sizes have been identified for the baseline processor, 64 and 36 points. Table 8 lists alternative implementations for these functions. The most efficient method in terms of hardware is to use a serial processor consisting of a memory and arithmetic unit with a controller

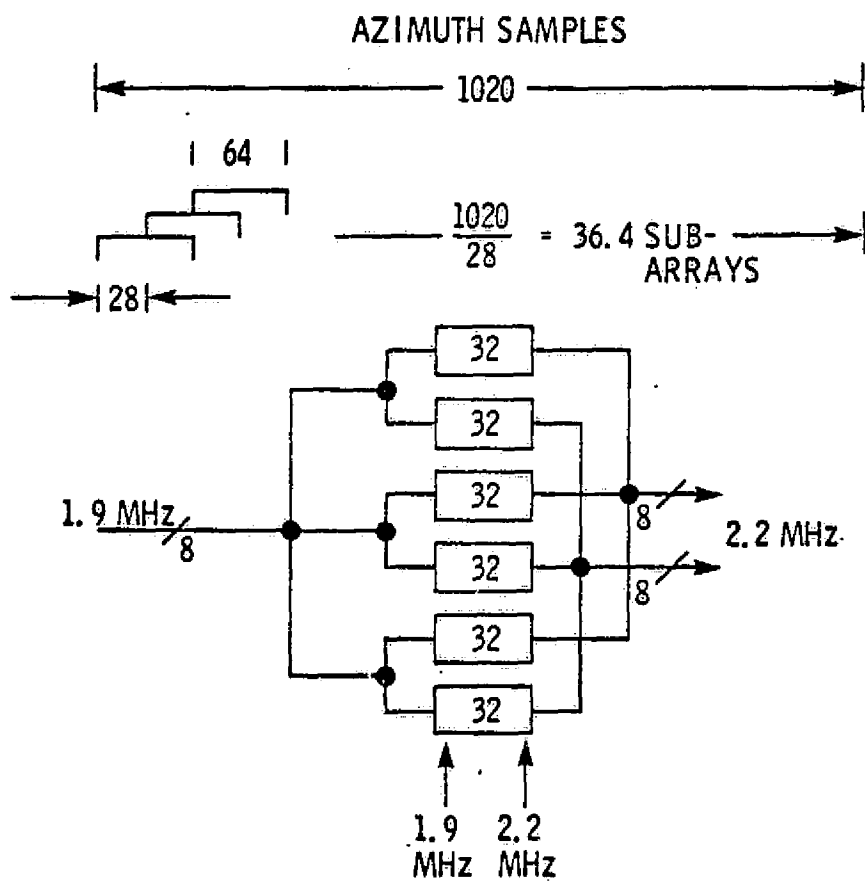


FIGURE 29. SUBARRAY FORMATION

TABLE 7. MEMORY REQUIREMENTS (20 km SWATH)

FUNCTION	DATA THROUGH-PUT RATE	MEMORY SIZE	ADDRESSING ALGORITHM	RAM IC SIZE	TOTAL RE-QUIRED	TECHNOLOGIES	POWER EST
PRF BUFFER	IN ≤ 23 MHz OUT - 1.9 MHz	DOUBLE BUFFER 1,152 WORDS BY 12 BITS	DELAY LINE DOUBLE BUFFER	1K X 4	6	CMOS/SOS	-
CORNER TURN- ING MEMORY	1.9 MHz	(1,152 X 1,020) 1,175,040 W X 12 BITS	FULL COR- NER TURN - SINGLE UNIT	16K X 1	861	MOS DYNAMIC	300 W
				65K X 1	216	MOS DYNAMIC	75 W
OVERLAP BUFFER	2.2 MHz	BUFFER 32 X 6 X 8	STORE - DELAY TWO CLOCKS	16 X 16	6	CMOS/SOS	-
COARSE RANGE MIGRATION	2.2 MHz (RADIX-2)	$\leq 1,020$ X 32 X 16	REORDER- ING ON BEAM - RANGE BASIS	16K X 1	32	MOS DYNAMIC	16
DATA ORDER- ING & INTER- POLATION	2.2 MHz	FIVE 36 X 64 X 16	DIAGONAL- IZATION OF SUBARRAYS	1K X 8	30	NMOS	7.5
OUTPUT SELECT	2.2 MHz	DUAL 16 X 20	DELAY- STORE, TWO CLOCKS	16 X 16	4	CMOS/SOS	-
LOOK INTEGRATORS	1.9 MHz	QUAD 255 X 1,024 X 10	RECIRCUL- ATE DATA	16K X 1	640	MOS DYNAMIC	150
				65K X 1	160	MOS DYNAMIC	40
TOTALS (EXCLUDING CONTROLS) USING 16K RAMS = 1,579 IC'S (500W) USING 65K RAMS = 454 IC'S (150W)							

to direct the computational sequence. Pipelining generally reduces the hardware but some algorithms such as the mixed radix and prime factor transforms which have been identified for the 36 point requirement do not readily lend themselves to an efficient pipeline. Therefore, while the net clock rate required of a radix-2, 32 and 64 point pipeline is one half the input sample rate the clock rate for the non-binary transform approaches is 3 to 4 times the sample rate.

TABLE 8. TRANSFORM ALTERNATIVES

DFT ALGORITHM	COMPLEX OPERATIONS PER TRANSFORM	SERIAL PROC CLOCK RATE	PIPELINING		PROCESSOR CHARACTERISTICS
			METHOD	CLOCK RATE	
32 POINT RADIX-2FFT	160	$2.5 f_s$	5 STAGES	$f_s/2$	ONE ARITHMETIC UNIT DESIGN
64 POINT RADIX-2 FFT	384	$3 f_s$	6 STAGES	$f_s/2$	- MEMORY AND PHASE REFERENCES VARY FROM STAGE TO STAGE - RATE REDUCTION OF TWO BY USING RADIX-2 PROCESSING
36 POINT MIXED RADIX (3 X 3 X 4)	288	$8 f_s$	2 UNITS - TWO 3- POINT, ONE 4-POINT	$4 f_s$	- EFFECTIVELY RADIX-1 PROCESS - PROCESSING LOAD HEAVY FOR EACH PIPELINE UNIT
36 POINT PRIME FACTOR (4 X 9)	235	$6.6 f_s$	2 UNITS - 9 POINT, 4 POINT FFT	$3.3 f_s$	MULTIPLIES IN PRIME FACTOR ARE REAL WEIGHTS

This points out an important function in a step transform subarray processor. Maximum hardware efficiency is realized when the transform sizes are binary

numbers. Thus, if the system parameters can be adjusted to provide this result significant hardware savings may result. (See Section 2.4.2)

Options for implementing the 64 point FFT are shown in Table 9. If a 64-point FFT can be used for the second FFT, the same FFT can be used for both functions with its clock rate increased by a factor of two. This approach was selected for the baseline design.

TABLE 9. FFT OPTIONS

IMPLEMENTATION	CLOCK RATE	COMPLEX MULT*	COMPLEX ADDS
6 STAGE PIPELINE	2.2MHz	8	12
6 STAGE RADIX-2 IN-PLACE	15.4MHz	2	2
3 STAGE RADIX-4 IN-PLACE	5.5MHz	4	8
6 STAGE PIPELINE SERVING BOTH FFT'S	3.8MHz	8	12

* INCLUDING DERAMPING OR PHASE MODULATION MULTIPLIES

The 64 point input FFT can be used directly if the second FFT size is 64 points or 32 points. The number of points in the second transform is set by the overlap factor for the subarrays and the total length of the synthetic array. The overlap of 36 of 64 selected for the baseline design resulted in 36 points for the second transform. The 36 points can be augmented with 28 zeros to obtain a 64 point sequence which can be processed in a 64 point FFT. This results in a net increase in the number of output picture elements (pixels) which may improve

image quality at the expense of output data rate and storage requirements. A second alternative is to set the overlap at 32 of 64. This requires more careful design of the weighting function across the subarray as discussed in Section 2.2.2. However, with the overlap at 32 of 64 the number of points in the second transform becomes 32 and the 64 point transform unit can be used. In this case its size is set equal to 32 by bypassing one stage of the pipeline. Both transforms can be multiplexed through the FFT by operating stages 2 through 6 at twice the clock rate of stage 1.

A special floating point architecture⁽⁴⁾ developed by RCA is employed in the FFT's.

FIGURE 30. 6 STAGE PIPELINE FFT FUNCTIONS

The general structure of the FFT arithmetic unit is shown in Figure 31. A common exponent is used for both the I and Q words so that the complex multiply function only employs the mantissas. In addition, the exponents are not decremented and no effort is made to left justify words. Extensive tests at RCA have shown that this approach operates at virtually the same accuracy level as full floating point arithmetic of a given quantization level.

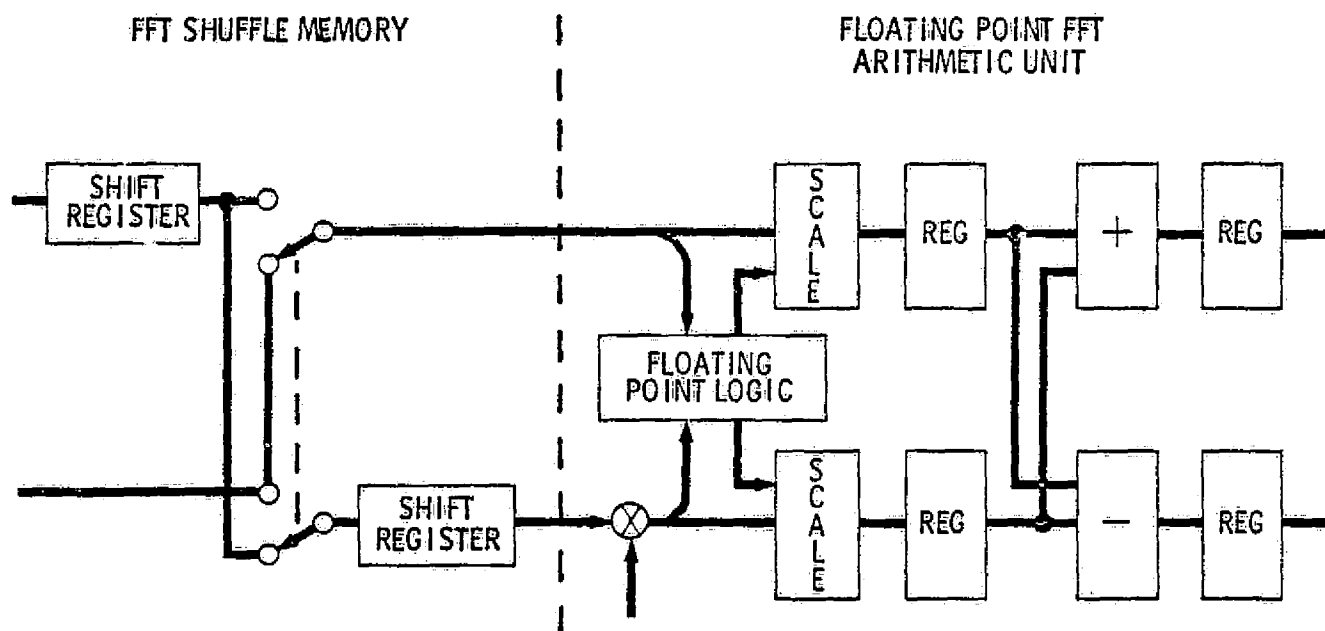


FIGURE 31. FLOATING POINT RADIX-2 FFT STAGE

Implementations of the FFT stage with four technology options are compared in Table 10. The first case is using a standard (no LSI) bipolar TTL logic implementation. A CMOS/SOS implementation with identical logic functions developed by RCA under contract to the Air Force Avionics Laboratory⁽⁵⁾ is

listed next. Another bipolar implementation employing currently available TRW 8 bit multipliers is next shown and finally a CMOS/SOS version using 16 x 16 CMOS/SOS RAM memories is given. The last case was used in the baseline hardware estimates.

TABLE 10. RADIX-2 FFT STAGE CIRCUIT COUNTS, EXCLUDING CONTROL

<u>IMPLEMENTATION</u>	<u>FUNCTION</u>			<u>TOTALS</u>
	<u>COMPLEX MULTIPLY</u>	<u>SCALE ADD/SUB</u>	<u>MEMORY, SW</u>	
TTL-MSI (9 BITS)	130	126	40	296
PWP CMOS/SOS (9 BITS)	9	13	22	44
BIPOLAR MSI/LSI (8 BITS)	50	100	40	190
CMOS/SOS USING 16X16 RAM MEMORY	9	13	9	31

2.3.2.5 Hardware Summary

A summary of a 20 km swath baseline SAR processor hardware is given in Table 11. In developing the table it was assumed that the circuits were packaged in leadless carriers and mounted on ceramic hybrid modules with an average of 30 circuits per module. The modules, measuring about 4 by 6 inches weigh 4 ounces each and a duplicate amount of hardware weight was assumed for interconnection and supporting nest structures for the modules.

TABLE 11. BASELINE ON-BOARD HARDWARE SUMMARY - 20 km SWATH

FUNCTION		CIRCUITS	POWER	WEIGHT	SIZE
MEMORIES	16K RAMS	1,579	500W MAX	-	-
	65K RAMS	454	25-150W		
ARITH PROCESSING		300	15W	-	-
CONTROL		200	30W	-	-
TOTAL	16K RAMS	2,079	545W MAX	15.8 kg	15,000 cm ³
	65K RAMS	954	70-195W	7.2 kg	7,500 cm ³

2.4 ALTERNATIVE PROCESSOR STUDY RESULTS

2.4.1 Variations of SAR Radar Parameters on Subarray Processing

Signal processing requirements were determined based on the various mission requirements supplied by JPL.

Table 12 lists these results. The baseline system is listed at the bottom of the table for comparison. The minimum and maximum subarray sizes were determined based on a maximum differential range walk of 0.5 range cells and a rotational range walk of ± 0.5 range cells. In all the cases, except the 10 meter, L band system, the required minimum subarray size was smaller than the required maximum size. This means that the basic approach considered for the baseline will apply with different processing parameters such as processing rate and subarray size. A baseline processor with sufficient programmability will handle all of the cases with the one exception.

The 10 meter, L band case requires an additional pre-filtering to split the antenna beam in half, separating the range migration effects into two parts. This enables the maximum required subarray size to be doubled. The implementation after pre-filtering will be the same as before. The implementation for the 10 meter, L band case is shown in Figure 32.

TABLE 12. SUBARRAY CONSTRAINTS FOR VARIOUS MISSION REQUIREMENTS

RESOLUTION	FREQ. BAND	BAND WIDTH (MHz)	COHERENT INT. TIME (SEC)	NO. OF SAMPLES/LOOK	RANGE WALK (CELLS)	MINIMUM SUBARRAY (PULSES)	MAXIMUM SUBARRAY (PULSES)	PREFILTER REQUIREMENTS*
10m	L	42.6	1.64	2698	184	108	59	2
	C		.40	658	45	6	244	-
50m	L	4.0	.59	970	49	29	360	-
50m	L	8.52	.46	756	83	48	133	-
50m	L	8.52	.33	542	58	35	185	-
75m	C	5.7	.053	87	10	1	3438	-
200m	L	1.2	.0545	83	5	3	2612	-
25m (BASELINE)	L	18.7	.646	1062	128	19	86	-

* REQUIRED WHEN MIN > MAX SUBARRAY

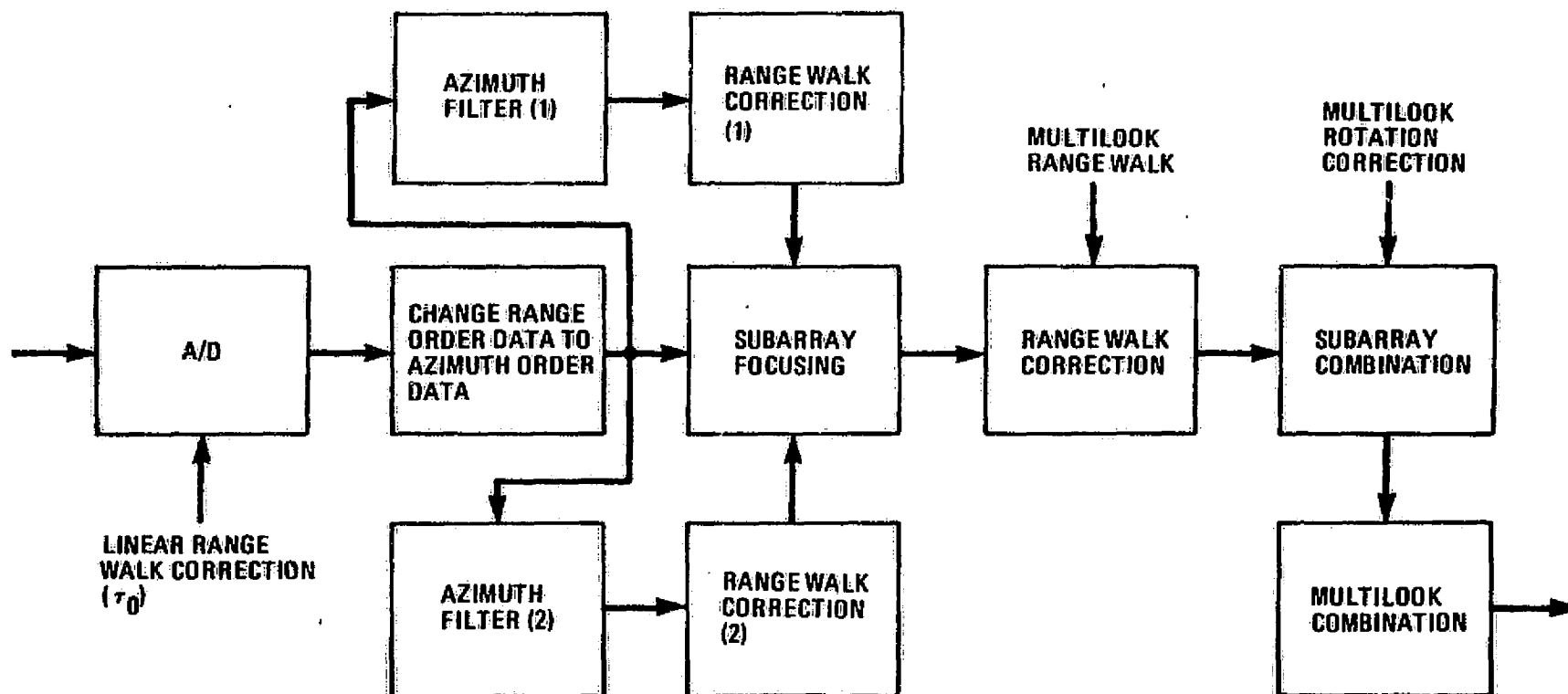


FIGURE 32. BLOCK DIAGRAM OF AZIMUTH PROCESSING FUNCTIONS WITH 2 PRE-FILTERS

2.4.2 Variations in Implementation of Step Transform Processing

2.4.2.1 General Programmability of Step Transform Processor - A general objective of the implementation of the SAR processor is that the basic design architecture be suitable for a wide variety of SAR applications. This would enable a given SAR processor to be used for a variety of system tasks. In addition, it may be desirable to scale a processor design for a particular resolution.

The same basic elements are used in the step transform SAR processor for virtually all system configurations. As the requirements change, however, the size, speed and control requirements of each element change. This is illustrated in Figure 33. The FFT processors are easily programmed to vary the length of the Fourier transform, in binary steps. For example, the PWP FFTs (reference 5) are programmable for 16, 32 and 64 points. On the other hand, while the memory functions are identical from system to system, the programmable control technique responding to system level inputs is desirable. Such an approach has been developed by RCA for the corner turning memory requirement as was discussed in Section 2.3.2.

The most complex memory control requirements occur in the range compensation function. The particular range compensation can be expected to vary during operation and the control for this memory must, therefore, adapt to these changing requirements. Because of the large storage required if discrete compensation conditions were stored, it is most appropriate to have the memory controls derived off-line in a microprocessor in anticipation of changing needs.

The varying SAR parameters can be expected to have general effects on the subarray processing requirements given constant SAR image requirements.

Radar Frequency

If the radar antenna is fixed in size, as the antenna frequency is increased,

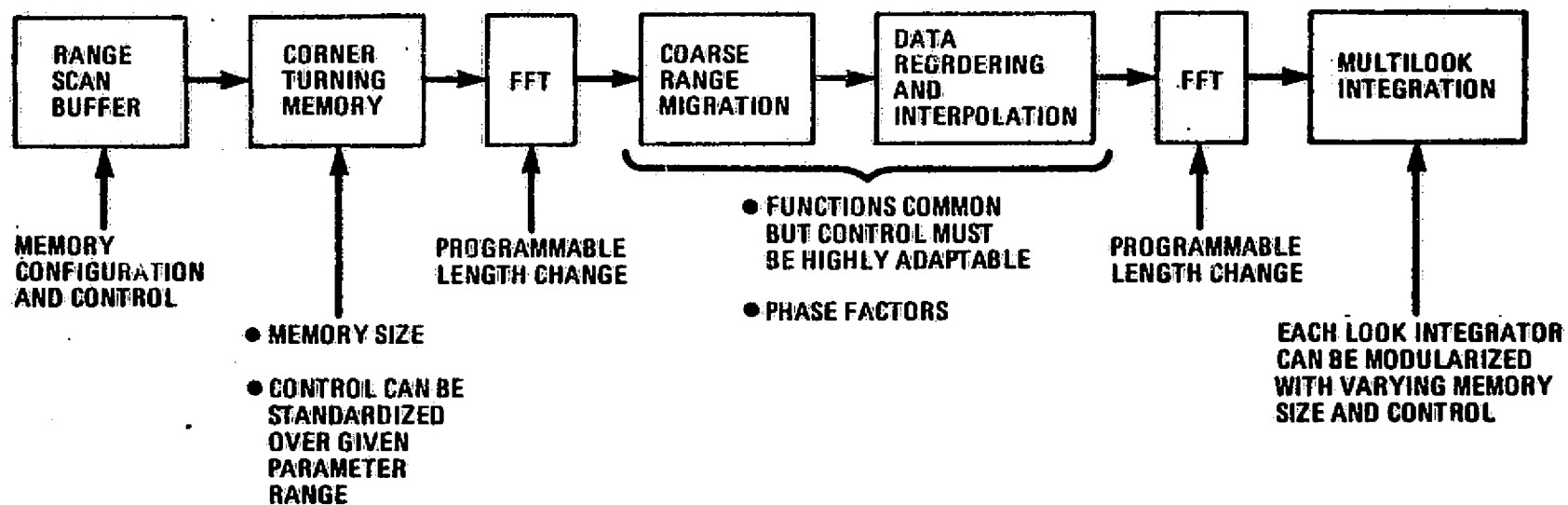


FIGURE 33. PROGRAMMABILITY OF BASELINE PROCESSOR DESIGN

one can expect that there will be less integration time ($T = R\lambda/2v\delta_A$) and hence less range walk. Since the minimum PRF is independent of frequency (min PRF = $\frac{2V}{D}$) the PRF will be constant. The net result is that the processing should be easier due to the reduction in range migration.

If the radar frequency is increased while holding the radar beamwidth fixed, the PRF will increase in proportion to f since $\theta \approx \lambda/D$. The integration time will decrease but the number of pulses will be constant since $N = \text{PRF} \cdot T$. The range walk will remain constant relative to a full beamwidth and the net result is that the processing complexity will remain constant with radar frequency.

Range and Azimuth Looks

As the number of range looks or operating frequencies are increased, the processing requirements will increase accordingly since one complete processor is required per range look.

As the number of azimuth looks increase, the image resolution (all other parameters remaining constant) will decrease in proportion but the processor load will stay approximately constant. The output data rate decreases.

Swath Width

The processing requirements will be virtually proportional to swath width since the number of data points to be processed per unit time will increase in proportion. The SAR processor can be modularized in segments of a total required swath width.

Incidence Angle

As the incidence angle increases, the required radar bandwidth decreases and the range coverage increases. It follows that the range migration will decrease ($\ddot{R} = v^2/R$). The maximum subarray size will then increase, the integration time

increases ($T = \frac{R\lambda}{2v\delta_A}$) and the minimum PRF will be constant. The processing load is reduced primarily from the bandwidth change. Large incidence angles could also result in a need for multiple elevation beams.

Sidelook Angle

As the sidelook angle changes from 90° in either direction, the range and range rate will increase. There will be a greater need for R correction at the A/D converter.

Altitude

An increase in altitude will increase the range and require more signal integration for a given signal-to-noise ratio.

Dynamic Range of Target Response

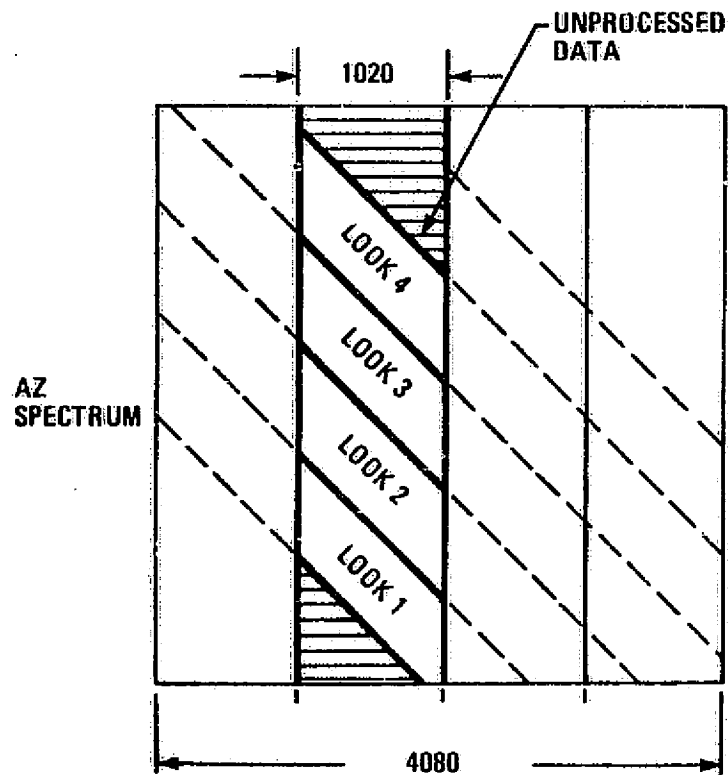
If the dynamic range of the target were to change from 25 dB to 100 dB as called out in Table 4 of the specifications, and a linear response were desired, the first effect would be on the A/D converter quantization bit requirements. Each increase in input dynamic range of 6 dB adds one bit to the A/D converter. Naturally, the increased input word size can be expected to also increase the word size in the processor. However, in many signal processing applications, and this should be particularly true in image processors, a very large dynamic range cannot be displayed due to contrast limitation. It therefore seems reasonable to implement a wide dynamic range SAR image processor with floating point arithmetic. This would have the result of maintaining a fixed accuracy level in the processor over varying dynamic range. The size of the processor would then remain essentially constant for all levels of dynamic range.

2.4.2.2 Multi-Look Batch Versus Continuous Strip Processing - The baseline processor is in essence a batch processor accepting a given window of data

and processing it to obtain the radar image. However, the scanning SAR is constantly in motion and unless some of the data, at the edges of the beam, is discarded, a full quality image will not be obtained across the image field. Each exposed image point must be integrated over the full coherent time of the array in order to obtain full resolution. In a batch processor, about 20 percent of the beam coverage is not integrated in the four-look case as shown in Figure 34(a). That is, the beam coverage must be 25 percent larger than that required for the actual integration time employed. If the data could be processed in a sliding aperture (continuous strip) processor, this loss in efficiency could be removed.

The integration patterns for a continuous strip multi-look SAR processor are shown in Figure 34(b). Each output image point is formed by an independent integration along a four look integration line. An implementation of this process can be accomplished in a subarray processor as indicated in Figure 35. All of the basic processing elements are employed.

BATCH PROCESSING



CONTINUOUS STRIP

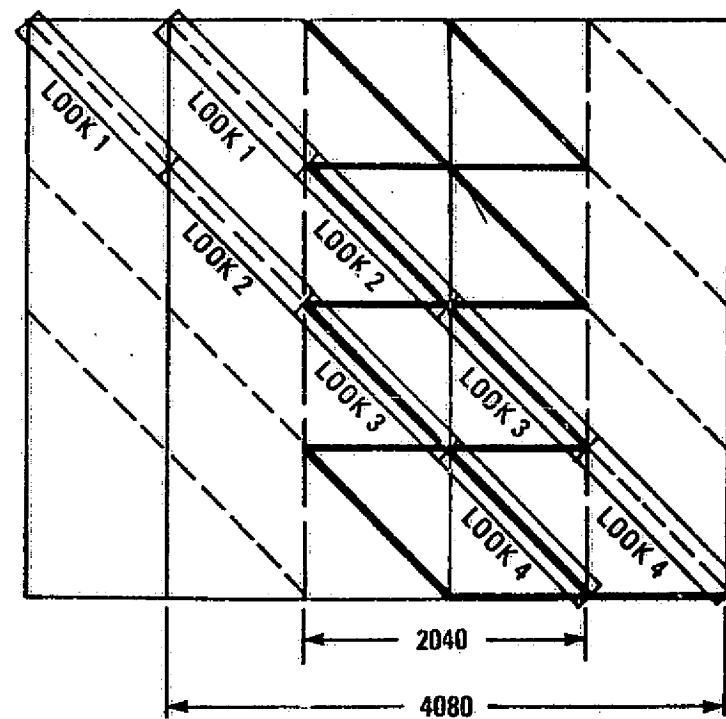


FIGURE 34. MULTI-LOOK SPECTRUM COVERAGE

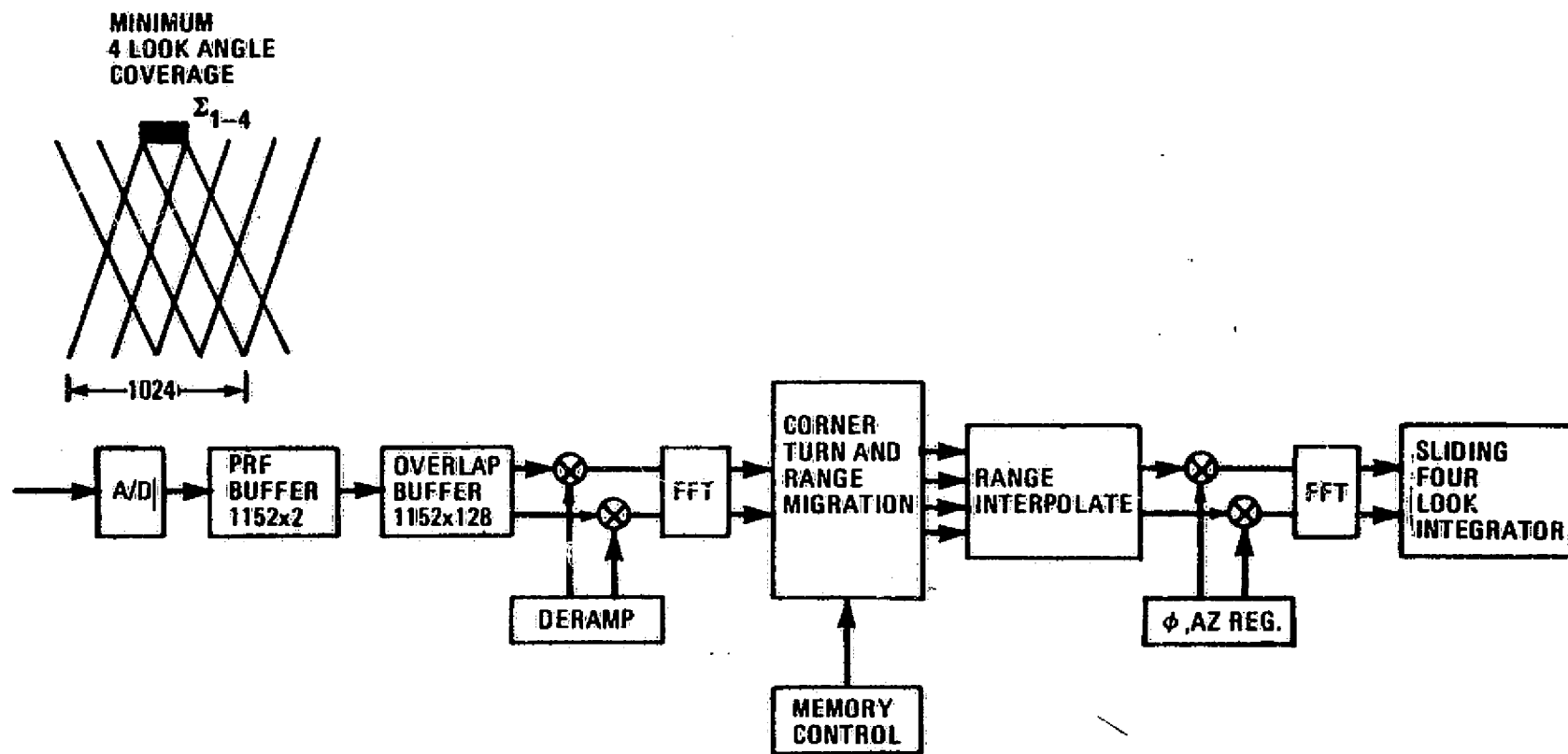


FIGURE 35. CONTINUOUS STRIP MULTI-LOOK PROCESSOR

The formation of subarrays prior to corner turning and the need to combine looks along diagonal paths has a major impact on memory management. The number of signal samples encompassed by the corner turning memory is increased by the overlap factor in the subarray formation. This is nominally about 2.28. In addition, since the integration must proceed along a diagonal path, the number of azimuth samples which must be stored will depend upon the efficiency of the memory. Figure 36 is a detail of a portion of Figure 34(b) and plots the azimuth spectrum versus azimuth samples for one range cell. At time t_1 , enough data has been received to allow coherent integration for Look 4 along the path indicated by the dark line. All of the spectral data to the left of the line has been used and can be discarded. The minimum storage is approximately one-half of the 36 subarrays by 16 spectral sample region for each look. This quantity multiplied by 4 looks and 1152 range cells gives a corner turning memory (perhaps more appropriately called a diagonalizing memory) a size of 1.33×10^6 words. This is only about 13% larger in words than the batch processor memory. However, an efficient implementation may be difficult to achieve. A sliding four-look integrator is also required. The integration must be accomplished over four diagonal patterns as shown in Figure 34(b) at intervals of 1020 range samples.

Techniques have been developed^(5,6) for efficient diagonalization of data using random access memories or shift registers. However, the referenced efforts dealt only with data of modest size and did not deal with a third dimension (range in this case). The diagonalization is also complicated by a non-ordered spectrum received from the pipeline FFT on two parallel (radix-2) lines. The difficulties of handling range migration in a continuous strip processor are illustrated in Figure 37. With no range migration, the full integration can always be obtained across the 36 subarrays spanning a single look within the

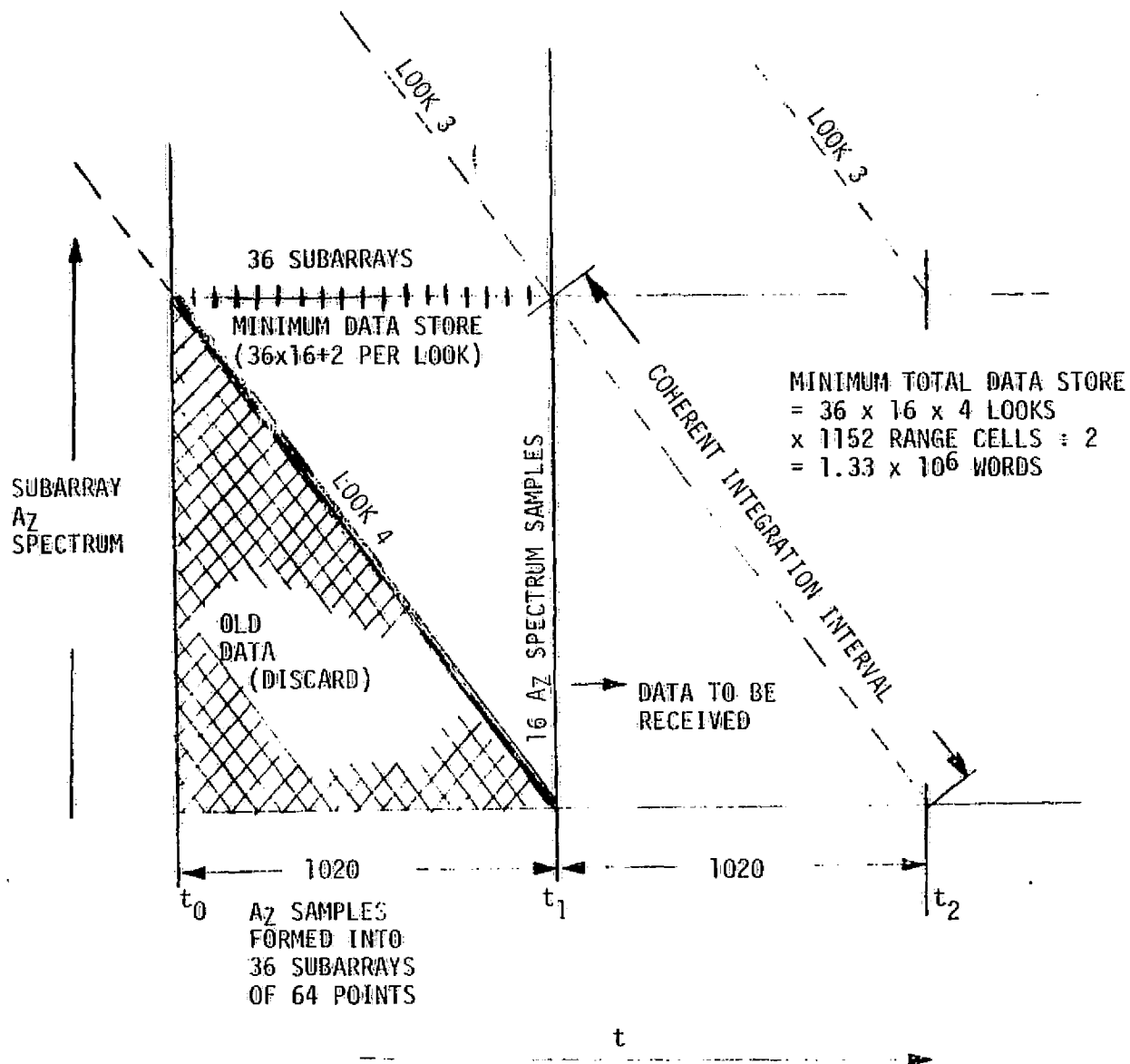


FIGURE 36. DIAGONALIZATION OF CORNER TURNING MEMORY FOR CONTINUOUS STRIP MAP PROCESSOR

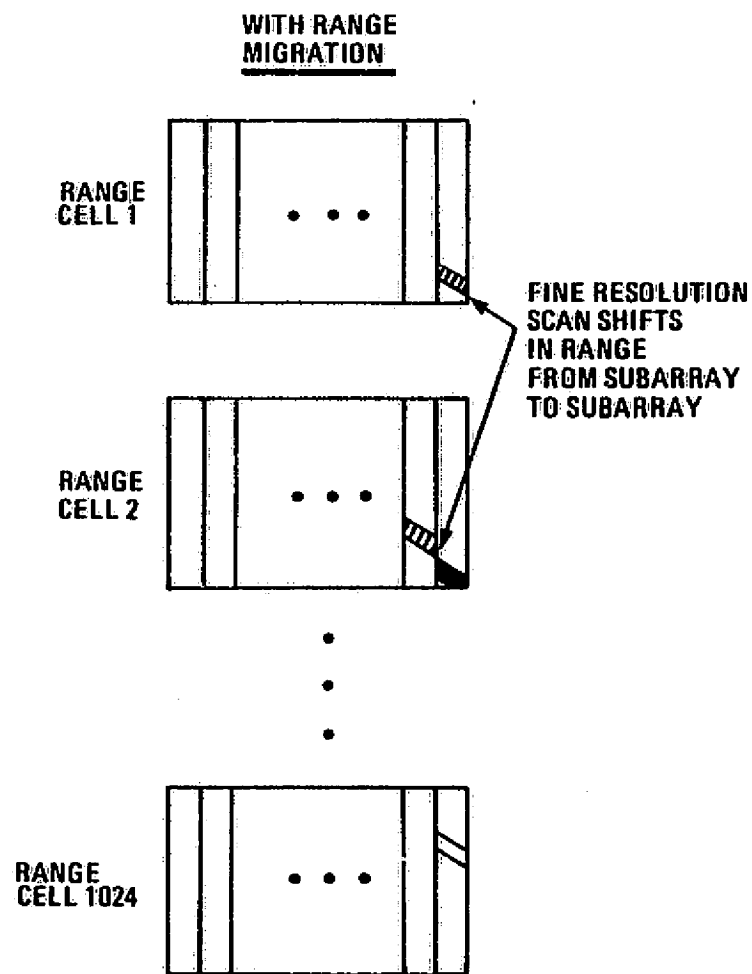
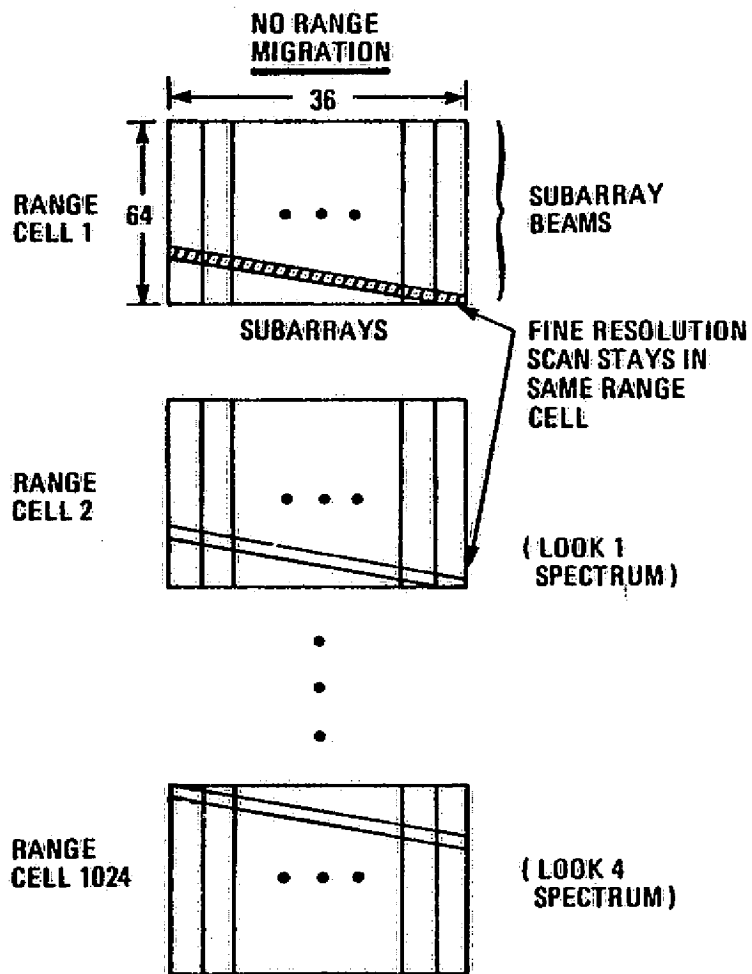


FIGURE 37. CONTINUOUS STRIP MEMORY READ-OUT SEQUENCE

same range cell. However, with range migration present, the fine resolution scan must shift from range cell to range cell across the subarrays. To achieve the required multi-dimensional programmability while maintaining a minimum memory size in the processor will be difficult. It may be possible to trade off simplification of the memory control for memory size. This trade-off may be especially attractive in the future as the density of digital memory circuits increases.

3.0 STUDY RESULTS, CONCLUSIONS AND RECOMMENDATIONS

This initial study was to configure a step transform processor for a set of given baseline system requirements and to assess the effect on the processor design of changing SAR radar parameters. The key accomplishments, conclusions and recommendations of the study for further work are listed below.

Accomplishments

- Completed overall baseline system design using step transform subarray technique.
- Developed procedures for adapting step transform processing architecture for varying SAR applications.
- Developed new mathematical analysis of step transform algorithm providing closed form expression for output.
- Computed performance level of baseline step transform processor.
- Conducted baseline hardware design for on-board processor.
- Developed step transform approaches for varying SAR radar parameters.

Conclusions

- Step transform subarray processing is a viable approach for processing the baseline SAR system.
- Memory components comprise by far the largest share of the hardware.
- Resolution achievable in SAR image with baseline range walk compensation technique is within two percent of theoretical.
- The baseline subarray approach can be used for all but highest resolution (10m) SAR cases. Variation of baseline will accommodate high resolution.

- A requirement for continuous strip map processor increases the complexity of the corner turning memory control.

Recommendations

With objective of implementing either ground or on-board processor, the following tasks are recommended as next step:

- Detail design and system simulation including specific hardware quantization effects and system control inputs.
- Exercise system simulator with real (Seasat) SAR data to verify processor design.
- Develop system hardware specifications.

With the objective of defining standardized SAR processor architecture, the following tasks are recommended:

- Develop detailed designs for programmable SAR functional units meeting future SAR system needs.
- Develop programmable control techniques.
- Validate performance via simulation.

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